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IMPROVED ANALOG TO DIGITAL CONVERTER CIRCUITS USING CMOS TECHNOLOGY

submitted by Wilfried Tenten for the degree of

Doctor of Philosophy (Ph.D.) of the University of Bath

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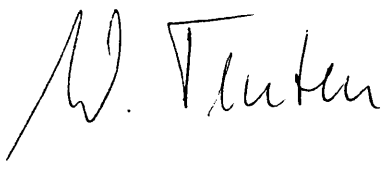
The work presented in this thesis was wholly undertaken while the candidate was registered as a part time student for the degree of doctor of philosophy at the University of Bath.



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This Ph.D. work is dedicated to my family.

C O N T E N T S

LIST OF SYMBOLS

A 1. Subthreshold current parameter

2. Gain of a transistor

3. Gain factor

4. Gain of the chopper amplifier

A0 DC-gain

ADNF AD-converter noise figure

A_M Gain of the main amplifier

A_N Gain of the nulling amplifier

A_n Gain of a multistage auto zero comparator

A_{dm} Differential mode gain

A_{PS} Power supply gain

A_{dyn} Gain of a dynamic OTA

A_{OTA} Gain of an OTA

B Geometry factor of Swanson and Meindl

B0 Conductivity constant

B0-BN Binary weight

C Capacitance

C' Geometry dependent capacitance

C1-4 Capacitance value for C1 to C4

CNF Comparator noise figure

CMRR Common Mode Rejection Ratio

C_D Depletion capacitance (space charge region)

C_H Auxiliary capacitance

C_L Load capacitance

C_X Circuit input capacitance

C_{DB} Drain bulk capacitance

C_{FB} Flat band capacitance

C_{HF} High frequency minimum capacitance

C_{LF} Low frequency minimum capacitance

C_{SB} Source bulk capacitance

C_{FS} Fast surface state capacitance

C_{GB} Gate bulk capacitance

C_{GD} Gate drain capacitance

C_{GS} Gate source capacitance

C_{ov} Overlap capacitance

C_{ox} Oxide capacitance

C_{ox} Oxide capacitance per unit area

C_{inp} Input capacitance

C_{load} Load capacitance

C_{ovn} Overlap capacitance of a n-channel transistor

C_{ovp} Overlap capacitance of a p-channel transistor

$\vec{D}$ Electrical displacement

DLE Differential linearity error

DNL_i Differential nonlinearity of the i-th level

E Full scale voltage value of an ADC

$\vec{E_S}$ Electrical field intensity

E_i Electron energy of the Fermi level in intrinsic material

E_C Energy of bottom of conductance band

E_{Cox} Energy of gate oxide

E_V Energy of top of valence band

E_F Energy of Fermi level

E_G Saturation electrical field intensity

E_g Semiconductor band gap voltage

e Euler's number

e_r Relative noise factor

e_{nc} noise voltage generated by the comparator

e_{ns} noise voltage of the source or network resistor

F 1. Correction factor of K2

2. Sample frequency

F_i Process dependent noise constant

f Frequency

f_0 Fundamental frequency

f_s Sample frequency

f_{cf} Corner frequency of the signal amplifier

f_{ch} Chopper corner frequency

$f_{pol,0}$ Pole frequency

G Conductance

g_m Transconductance

g_{BS} Substrate conductance

g_{DS} Channel conductance

H Transfer function

$\overline{H}$ Magnetic field intensity

H_z Transfer function of the z-domain

H_{OTA} Transfer function of the OTA

h Quantisized Planck constant

I Current

I Magnetically induced current

INL Integral Nonlinearity

$I_{+,-}$ Positive/negative OTA input current

I_0 Reference current

I_B Bias current

I_L Load current

I_D Drain current

I_{CM} Common mode current

I_{D0} Weak inversion current

I_{DS} Drain source current

I_{Bias} Bias current

I_{out} Output current

SYMBOLS

$I_{ovn,p}$ Overlap current

I_{ref} Reference current

i_D Drain current variation

K ADC gain factor

K1 Backbias constant

K2 Channel length modulation constant

K_F Flicker noise coefficient

k Boltzmann constant

k_i Frequency dependent noise constant

L Transistor length

L Inductance

L' Geometry dependent inductance

L_D Correction of the channel length

L_R Energy of a binary step

L_{DB} Debye length

$L_{N,opt}$ Optimized n-channel transistor length

LSB_{ADC} Least significant bit of an ADC

l_r Step width of voltage axis

N Concentration of majority charge carriers in doped silicon zones

N_A Concentration of acceptor charges (n-type material)

N_B Density of substrate doping

N_D Concentration of donor charges (n-type material)

N_{eff} Effective bit range

n Slope factor

n Free charge carrier concentration for minorities

n_i Free electron concentration in intrinsic silicon

p Free charge carrier concentration for majorities

PSRR Power Supply Rejection Ratio

Q Charge to load the output capacitance

Q Induced electric charge

SYMBOLS

Q_K Charge coefficient

Q_B Space charge per unit area

Q_S,Q_{SS} Charges within the silicon surface

q Charge

q LSB quantum

q_{ft} Clock feed through charge

q_{Vi} Charge of the input capacitance

q_{CH} Charge of the auxiliary capacitance

R Resistance

R_L Load resistance

R_{on} Symmetric transfer-gate on resistance

R_{Bias} Bias transistor resistance

r Resolution of an ADC

r_{on} Channel on resistance

r_{out} Output resistance

r_{trn} Resistance of the output transistors of an OTA

$\vec{S}$ Pointing vector

S1 Total input power spectrum

S2 Average value of the output power spectrum

SNR Signal noise ratio

SQR Signal quantization ratio

S_R Slew rate

S_{no} Noise power of the base band

S_{fold} Noise spectrum of the folding terms

$S2_{1/f}$ 1/f input power spectrum

$S2_{kT/C}$ thermal input power spectrum

S_{rms} Spectral density of a full scale sine wave

T 1. Absolute temperature

2. Time period

TO Absolute temperature 273K

SYMBOLS

T_K Comparison time

τ time constant

T_{SC} Switched capacitor period time

t Time

t_{ox} Oxide thickness

V MIS potential

Va Voltage after the time step

Vb Voltage before the time step

V_B 1. Bulk voltage

2. Bulk Fermi potential coefficient

V_D Drain voltage

V_G Gate voltage

V_{HL} Semiconductor contact potential

V^2_N Equivalent noise voltage

V_S Source voltage

V_S Surface potential coefficient

V_T Threshold voltage

V_{Bi} Voltage of the i-th level

V_{Bi-1} Voltage of the (i-1)th level

V_{BS} Bulk source voltage

$V_{C1,2}$ Voltage across C1/C2

V_{CH} Voltage across the auxiliary capacitor

V_{CT} Voltage across the top plate parasitic capacitance

V_{CX} Voltage across the input capacitance

V_{DD} Positive supply voltage

V_{DS} Drain source voltage

V_{GS} Gate source voltage

V^2_{NO} Equivalent noise voltage of an amplifier stage

V^2_{NR} Equivalent noise voltage of a resistor

V^2_{NT} Equivalent noise voltage of a transistor

V_{T0} Threshold voltage at $V_{DS} = 0V$ and $V_{BS} = 0V$

V_{Bias} Bias voltage

V_{Clb} Voltage across input capacitor

V_{cin} Input voltage of the ac cross coupled comparator

V_{DSS} Negative power supply voltage

V_{err} Error voltage

$V_{GSn,p}$ N,p-channel transistor gate-source voltage

$V_{inn,p}$ Negative/positive input voltage

$V_{N,N,P}^2$ N,P-channel transistor equivalent noise voltage

V_{off} Offset voltage

$V_{out,1,2}$ Output voltages

V_{ref} Reference voltage

V_{CX} Gate input voltage

V_{CLft} Clock feed through voltage

V_{Geff} Effective gate source voltage

V_{Step} Voltage of an ADC step

$V_{out,EVIS\,2}$ Output voltage of a VIS reference

$V_{clock\,n,p}$ Clock voltage at the gate of a n/p-channel transistor

$V_{eff,sine}$ Effective voltage of a sinusoidal wave

$V_{GS,eff}$ Effective gate source voltage

$V_{Geff\,inp}$ Effective input voltage

$V_{off,eff}$ Effective offset voltage

$V_{off,OTA}$ OTA offset voltage

V_{out} Output voltage

$V_{inp+,-}$ Positive/negative input voltage

$V_{inp,Amp}$ Amplifier input voltage

$V_{ref,Amp}$ Amplifier reference voltage

$\overline{v}$ Noise voltage

W Transitor width

W_i Spectral energy within the passband

SYMBOLS

W_s Spectral energy of the fundamental frequency

W_{sa} Energy before charge distribution

W_{sb} Energy after charge distribution

X Auxiliary variable

X1 1/f noise coefficient

X2 Thermal noise coefficient

Y Auxiliary variable

y analogue slope value within a time interval T

Z Auxiliary variable

Z Impedance

α Channel length modulation parameter

α Damping constant

α Nonideality constant of a VIS reference circuit

β Transistor specific conductance constant

β_0 Transistor specific conductance constant (25 deg.)

$j\beta$ Phase constant

γ Propagation constant

λ Wave length

$\delta(t)$ Dirac pulse

$\overline{\varepsilon^2}$ Quantisation error

$\varepsilon_{l,u}$ Lower, upper ADC error voltage

$\varepsilon_{ADC,DAC}$ error of an ADC,DAC

ε_{ox} SiO_2permittivity

μ_r Mobility ratio of the free charge carriers

ρ ACF of a noise emitting resistor

τ Time constant

Φ Magnetic flux

Φ_F Bulk Fermi potential

Φ_M Metal to oxide work function

Φ_S Surface inversion potential

SYMBOLS

Φ_{MS} Metal to silicon work function

Φ_{SO} Silicon to oxide work function

Ψ auxiliary name for a complex plane

Abstract

In shifting the resolution of analogue to digital converters to the 16 bit range, new techniques to improve the quality of the building blocks and new ways to produce reference voltages of high quality are proposed. Using chopper techniques, two different one-stage amplifiers with high gain are presented. One amplifier is single ended, the other fully differential. The next component improved by a new design technique is a fully symmetric capacitor cross coupled comparator. Based on these new chopper amplifiers, new reference sources are introduced that offer a staircase shaped reference voltage with up to 16 bit accuracy. The technique used for these new references is based on the voltage inverter switch (VIS) principle, which measures all error voltages before the charge redistribution. During the charge redistribution process, the measured and stored error voltage is added to the resulting voltage, so that charge sharing is very accurate. Six new analogue to digital converters are presented. The successive approximation technique, without the need of a succesive approximation register is introduced. An algorithmic ADC with a minimized number of components offers 14 bit accuracy. A Candy-type delta sigma ADC is then presented, that introduces the difference technique. Another method of achieving 16 bit accuracy is the incremental principle. This is used in conjunction with the difference delta-sigma principle, using the fully differential VIS concept. It is shown that the 16 bit range is achievable without the help of the delta-sigma principle if the VIS circuits combined with the incremental operation are used. All these ADCs offer the advantage that no special digital control blocks are required. Digital control may be done internally by using a minimal number of digital circuits.

CHAPTER 1

Introduction

The modern world requires more and more precision in communication electronics and other fields like medicine, sensor applications, automotive industries and instrumentation. The increasing preference is to use digital circuits, because of their stability against ringing on supply line, ringing or noise on data lines, and other effects, that can severly degrade analogue circuitry. For example during the last decade, a lot of work has been done on digital filtering. Fettweis [1] showed that wave digital filtering offers some improvements in the sensitivity of limit cycles. This trend has an effect on the interface world, i.e. interface circuits between the analogue time continuous spectrum, and the digital side which now require resolutions of better than 12 bits to fulfil the high quality demands for modern applications. Current techniques in industrial applications include the resistor string, the capacitor array and the delta-sigma technique. Resistor strings are limited in accuracy to about 8 to 10 bit, while capacitor arrays can be used up to 14 bit, if calibration techniques are used internally to stabilize the less significant bits. The sigma-delta principle offers the ability to use standard elements in the 12 to 14 bit range. The improvement of resolution is achieved here with the help of the noise shaping effect of the integrator and with the help of statistics. Voltage values are oversampled with a much higher frequency than the Nyquist frequency of the passband. Factors that limit the resolution of standard elements are mostly leakages produced during charge balancing, by the ringing of the power supply lines and by the limited gain of the amplifiers.

Improvements in the quality of the analogue to digital conversion process can be achieved by components whose parameters are closer to these quality demands than those of standard elements. Chapter three presents three new analogue building blocks

that fulfil the demands of analogue to digital converters for the 16 bit range. These new blocks are two chopper amplifiers based on the one stage operational transconductance amplifier (OTA) principle. One amplifier is single ended, the other one is a fully differential OTA. The signal path remains time continuous. The third new analogue building block is a new type of comparator. Based on the standard auto-zero inverter technique, a capacitor cross coupling technique offers a self controlled feed-forward technique. This new comparator technique shifts the resolution to 16 bit accuracy. Clock-feed through influences and power supply ringing are vastly reduced, because the design is absolutely symmetrical.

These new building blocks combine to produce high accuracy in analogue to digital converter (ADC) designs. The overall requirements for high quality ADCs are:

- proper component matching
- proper device matching
- proper reference voltage

Chapter five introduces a new way to create stable reference voltages. The reference voltages are produced with a voltage staircase characteristic. To produce a staircase which splits each voltage step by a factor of two to an accuracy of 16 bit, the charge distribution process must be monitored and controlled. This is achieved with the help of the voltage inversion switch (VIS) principle, first introduced by Fettweis for filter applications. Three VIS circuits are presented in chapter five: a voltage follower VIS (V-VIS), the integrator VIS (I-VIS) and the fully differential VIS (D-VIS).

Chapter seven presents six new analogue to digital converter (ADC) circuits. The techniques used are the successive approximation (without the need of a successive approximation register), the algorithmic principle, the incremental principle and the delta-sigma principle. Except for the algorithmic ADC, which needs no VIS control, all the ADCs are controlled by VIS circuits. It will be shown that the accuracy can now

be stretched to the 16 bit range without the need of a calibration circuit.

The operation of the building blocks was verified by simulation using a computer package called BONSAI. There was no simulation tool available that could simulate all the ADC with a lot of time steps. Therefore a simulator based on switched capacitor building blocks, a delay circuit, a summation and some digital logic was developed. This simulator (SC-program) was verified with BONSAI simulation results and with the results of the breadboarded VIS circuits. The analysis in the frequency domain was done with a multiradix FFT simulator (MURF).

The delta-sigma principle was introduced to allow higher accuracy with standard building blocks. Delta sigma converters published recently offer a resolution up to 14 bit. This is achieved by a multi-integrator technique. Normally these systems show instabilities if more than 2 integrators are used. On the other hand, improvements in accuracy can only be achieved by using more integrator stages. Therefore the MASH principle (this is a special sigma-delta ADC) was introduced. The MASH principle offers up to 14 bit.

It is shown in chapter eight, that the accuracy of the new ADC principles is in the 16 bit range, thus there is no need for the delta-sigma principle.

The parameter set used in this work is that of a standard 3um process. Due to company confidential rules, this parameter set cannot be published.

REFERENCES CHAPTER 1

[1] Fettweis A, "Wave Digital Filters: Theory and Practice", Proceedings of IEEE, Vol.74, No 2, pp. 270 - 285, Feb. 1986

CHAPTER 2

BASIC MOS THEORY

2.0 MOS Transistor Models

Field effect transistors are divided into depletion and enhancement transistors, depending on the structure of the channel. A depletion transistor has a low impedance channel region, that means charge carriers are present, even when the gate voltage is zero. Increasing the gate voltage means increasing the electrical field to control the channel, forcing a decrease in charge carriers and hence a decrease of the channel conductivity. Enhancement devices have a high impedance channel until a bias is applied to the gate draw charge carriers into the channel to form a conducting region.

Each type of transistor can be constructed using p- or n-channel devices. This is defined by the doping of the source and drain regions, n-type doping for n-channel p-type doping for p-channel.

The development of the circuits presented in this work is done using p- and n-channel enhancement transistors. The standard drawing for these MOS transistors is shown in figure 2.1.

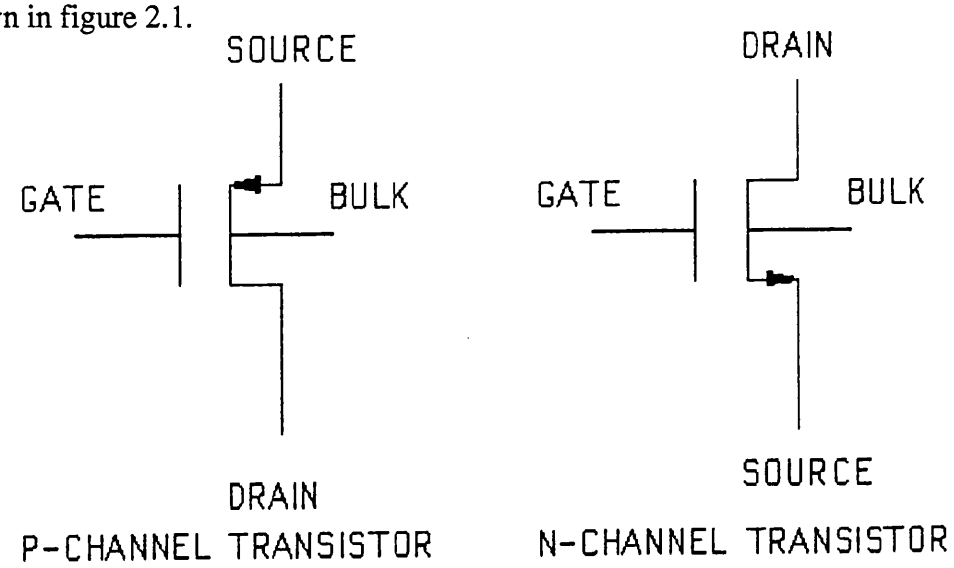

Figure 2.1 Drawing standards for MOS enhancement transistors

Figure 2.2 shows the cross sectional view of a MOS-FET transistor. The transistor width is labelled with W, the length of the transistor is labelled with L. The channel length modulation L_D, defined in section 2.2.4, is to be seen as a space charge region between the end of the transistor channel and the drain diffusion and is labelled with L_D. The gate, the drain and the source region is abbreviated with G, D and S, respectively. The gate oxide has the label tox. Figure 2.3 shows a plot of n-channel and p-channel transistor output characteristics.

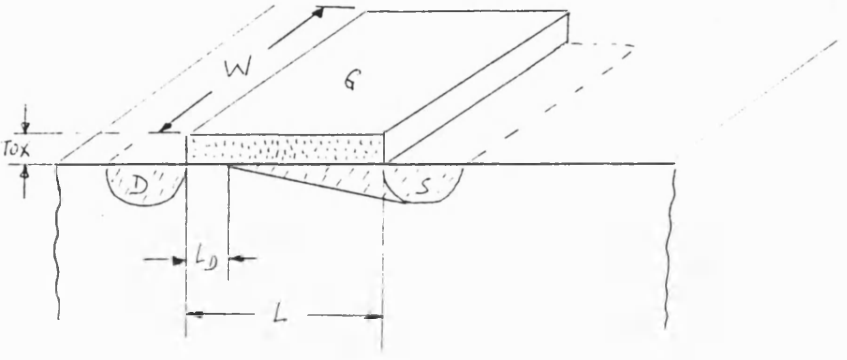

Figure 2.2 Cross sectional view of a MOS-FET

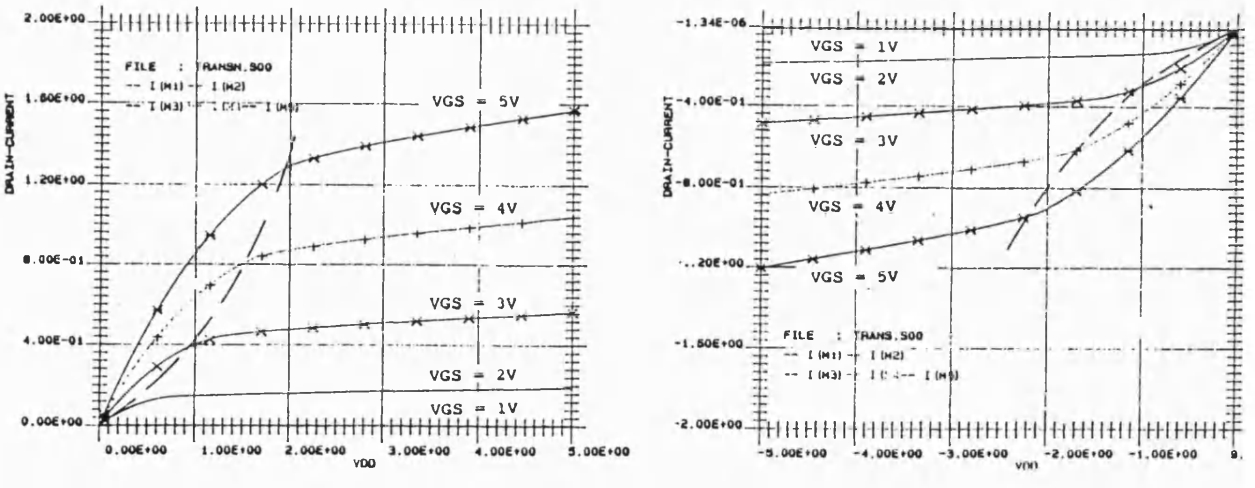

Figure 2.3 n- and p-channel transistor output characteristics

The action of MOS transistors is governed by the modulation of the source-drain current by the applied voltage on the gate. This action is described in a great many publications, ie. [1 to 12].

For analogue design we need to determine various parameters, in order to develop a suitable model for the device. The following section describes in some detail the most popular MOS model for enhancement devices, the gradual channel approximation. The model described here is implemented in a more sophisticated way in the network simulation package "BONSAI" [9]. BONSAI is used as a circuit development tool in this work. The weak inversion model presented in section 2.1 is not included in BONSAI.

Traditionally the literature splits the MOS transistor models into two operating regions depending on the density of mobile current carriers with respect to the fixed carriers within the channel. These regions are called the weak inversion and the strong inversion regions.

The operating area of a transistor depends on the gate control voltage. For an n-channel device, gate voltages less than 0V related to source, force an accumulation of holes at the Si-SiO_2 interface. This accumulation forces the gate capacitance to be directly connected to the bulk. Obviously the capacitance per unit area in accumulation mode can be written as:

$$C_{\underline{Ox}} = \frac{\varepsilon_0 \cdot \varepsilon_{Ox}}{t_{Ox}} \tag{2.1}$$

where: C_{Ox}: Oxide capacitance per area

ε_{Ox} : SiO_2 permittivity (≈ 3.7)

t_{Ox} : Oxide thickness

Depletion occurs within the gate voltage range from 0V up to the threshold voltage V_T. This forces a depletion of mobile majority carriers and induces a negative space charge region. The depth of this space charge region depends on the bulk doping and increases with the gate to bulk voltage. A voltage dependent capacitor connected in series with C_{Ox} is built by this space charge region. Increasing gate voltage results in an increase of minority carriers (electrons) at the Si-SiO_2 interface layer. The transistor is now inverted, a conductive layer, the inversion layer, is built up of electrons near the Si-SiO_2 interface. The gate voltage at which the space charge has the maximum depth is defined as the threshold voltage. Additionally the threshold voltage defines the interface between strong inversion, when there are induced inversion charges due to increasing gate voltage, and the weak inversion region at lower gate voltages that continues into the accumulation region at negative gate voltages. Therefore the weak inversion region is also called the subthreshold region.

2.1 Weak Inversion Model

The weak inversion region will be discussed first. This region was described by Swanson and Meindl [10] in early 1972. Vittoz and Fellrath completed the weak inversion theory in a series of papers published in the 70's and 80's [11] to [13]. Location of weak inversion is possible by plotting a C-V curve for the gate. The transfer characteristic passes through a minimum within weak inversion operation during a C-V low frequency measurement. This is shown on the graph in figure 2.4.

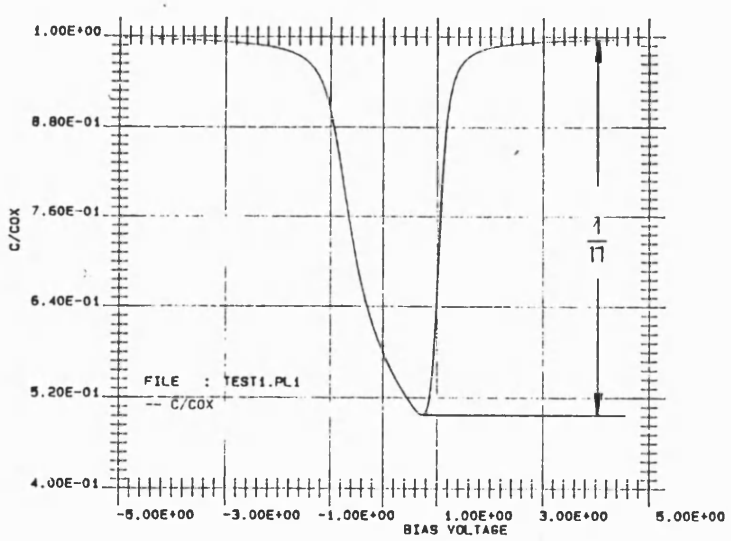

Figure 2.4 Weak inversion on a C-V curve

The threshold voltage lies within this transition region. The subthreshold drain current has an exponential dependence on the drain to source voltage as well as to the gate voltage. The charges of that drain current are mostly thermally generated. The potential barrier for the subthreshold current is defined as Φ_B and is controlled by the gate to source voltage.

$$\Phi_B = A \cdot (V_{GS} - V_{T0}) + B \cdot V_{DS} \tag{2.2}$$

where: A : subthreshold current parameter

B : geometry factor of Swanson and Meindl

V_{GS} : gate-source control voltage

V_{T0} : threshold voltage at V_{DS} = 0V and V_{BS} = 0V

$$A = \frac{C_{Ox}}{C_{Ox} + C_D + C_{FS}}$$

C_{FS} : fast surface state capacitance

C_D : depletion capacitance (space charge region)

$$B = \frac{\varepsilon_{Si} \cdot t_{Ox}}{\pi \cdot \varepsilon_{Ox} \cdot L}$$

The threshold voltage in weak inversion region (eqn. (2.3)) is dependent on the drain to source voltage V_{DS} and is a function of the parameters A and B.

$$V_T = V_{T0} - \frac{B}{A} \cdot V_{DS} \tag{2.3}$$

The parameter n in figure 2.4 is the slope factor. This slope factor is dependent on the capacitive voltage divider and can be described [14] as:

$$n = 1 + W \cdot L \cdot \frac{C_{Ox}}{C_D} \tag{2.4}$$

where: C_{Ox} is the oxide capacitance per unit area

The drain current for the weak inversion region can be expressed as [8]:

$$I_D \propto e^{\frac{\Phi_B \cdot q}{k \cdot T}} \tag{2.5}$$

The slope factor is nearly independent of the source potential and can be easily measured in any C-V plot.

The last relation is combined with the designed and measured transistor parameters in weak inversion. Vittoz gives in [14] a useful expression for the drain current in the subthreshold region:

$$I_D = I_{D0} \cdot e^{\frac{V_G}{n \cdot V_T}} \cdot \left(e^{-\frac{V_S}{V_T}} - e^{-\frac{V_D}{V_T}} \right) \tag{2.6}$$

The parameter I_{D0} in eqn. (2.6) is now discussed. I_{D0} can likened to the bipolar saturation current. As described in [14], the current I_{D0} show big variations in parameter measurement statistics. Hence design in weak inversion operation should be based on constant drain current and not on constant gate voltage as is usual in strong inversion.

Concerning weak inversion operation, this case only occurs during a clock period controlling voltage inverter switches (described in a later chapter). During this period an amplifier runs unloaded, and the transistors are forced to operate in the weak inversion. During the active phase, the transistors of the amplifiers operate in saturation. Dynamic control is achieved using the current of a capacitor, connected in series with a bias current mirror transistor.

2.2 Strong Inversion Model

The standard operating region in most analogue applications is within the strong inversion region, that means the gate voltage is above the threshold voltage. The current in strong inversion is drift current. Models for strong inversion are split into two operating regions:

1. linear region :
   terminated by the drain to source saturation voltage
2. saturation region :
   above the drain to source saturation voltage

In modelling strong inversion transistor behaviour, a number of effects must be considered. Two aspects are considered in the current work :

1. Evaluation of the circuit using a model suitable for implementation on a pocket calculator.
2. Development of more complex computer aided simulations based on the first step.

Models suitable for pocket calculator design must be relatively simple. The calculations are obviously less accurate than those done using computer packages. The most important equations are be derived from the gradual channel approximation (GCA) model described in [9].

2.2.1 Threshold Voltage

The drain current is controlled by the gate source voltage above the threshold voltage. The threshold voltage is defined as the required gate source voltage to achieve surface inversion, that means the charge density of mobile carriers within the channel is 0 if the threshold voltage applied on the gate. The threshold voltage is calculated from eqn. (2.7).

$$V_{T0} = \Phi_{MS} - \frac{Q_{SS}}{C_{Ox}} + 2 \cdot \Phi_F + \frac{\sqrt{2 \cdot \Phi_F} \cdot \sqrt{2 \cdot q \cdot \varepsilon_0 \cdot \varepsilon_{Si} \cdot N_B}}{C_{Ox}} \tag{2.7}$$

$$\Phi_F = \frac{kT}{q} \cdot \ln\left(\frac{N_A}{n_i}\right) \tag{2.8}$$

where: Φ_F : bulk Fermi potential

N_B : density of substrate doping

ε_{Si} : dielectric constant of Si

Φ_{MS} : metal to silicon work function of

N_A : concentration of acceptor charges (n-type material)

n_i : free electron concentration in intrinsic silicon

Q_{SS} : charges within the silicon surface

C_{Ox} : gate oxide capacitance

Figure 2.5 shows the band diagram of a MIS (Metal Insulator Silicon) structure in flat band condition as an example to clarify the various potentials in a MIS structure. Flat band condition means an equilibrium of the potential lines up to the interface boundaries.

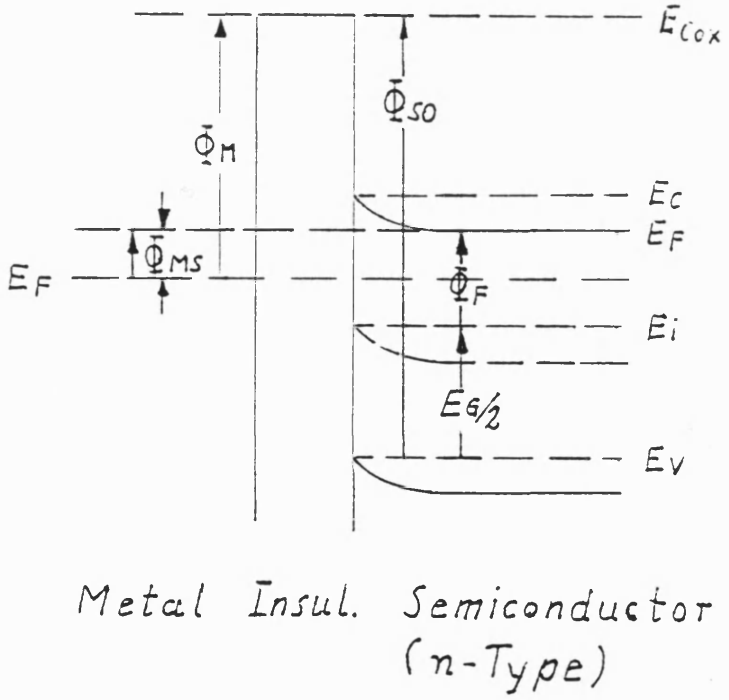

Figure 2.5 Energy Bands in Flat Band Condition

where:

E_i : Electron energy of the Fermi level in intrinsic material

E_{Cox} : Energy of gate oxide

E_V : Energy of top of valence band

E_F : Energy of Fermi level

E_C : Energy of bottom of conductance band

Φ_{MS} : Metal-Silicon work function

Φ_{SO} : Silicon to oxide work function

Figure 2.3 shows the drain current characteristic curves in the nonsaturated and the saturated region. The regions are divided by the channel pinch off parabola (dashed line).

2.2.2 Backbias Effect

Equation (2.7) can be rewritten [9] as:

$$V_{T0} = \frac{t_{Ox}}{\varepsilon_0 \cdot \varepsilon_{Ox}} \cdot (\sqrt{2 \cdot q \cdot N_B \cdot \varepsilon_{Si} \cdot \Phi_S} - Q_{SS}) \qquad (2.10)$$

where: Φ_S is the surface inversion potential

N_B is the density of dopants in bulk silicon

The potential difference between the source and the bulk is called the backbias. Increasing backbiasing forces the threshold voltage to increase also. The increase can be described as an additional term in the threshold definition of V_{T0}. The threshold voltage V_T including backbias is given by the following equation:

$$V_T = V_{T0} + \frac{t_{Ox}}{\varepsilon_{Ox}} \cdot \sqrt{2 \cdot q \cdot N_B \cdot \varepsilon_0 \cdot \varepsilon_{Si}} \cdot (\sqrt{\Phi_S + V_{SB}} - \sqrt{\Phi_S}) \qquad (2.11)$$

Equation (2.11) can be simplified to the expression used in BONSAI:

$$V_T = V_{T0} + K1 \cdot (\sqrt{\Phi_S + V_{SB}} - \sqrt{\Phi_S}) \tag{2.12}$$

The term $K1 \cdot (...)$ of eqn. (2.12) is the backbias influence. K1 is called the backbias constant or substrate bias constant.

$$K1 = \frac{t_{Ox}}{\varepsilon_{Ox}} \cdot \sqrt{2 \cdot q \cdot N_B \cdot \varepsilon_0 \cdot \varepsilon_{Si}} \tag{2.13}$$

The following figure shows a BONSAI simulation of a I_{DS} versus V_{GS} plot, in which the backbias voltage is the variable.

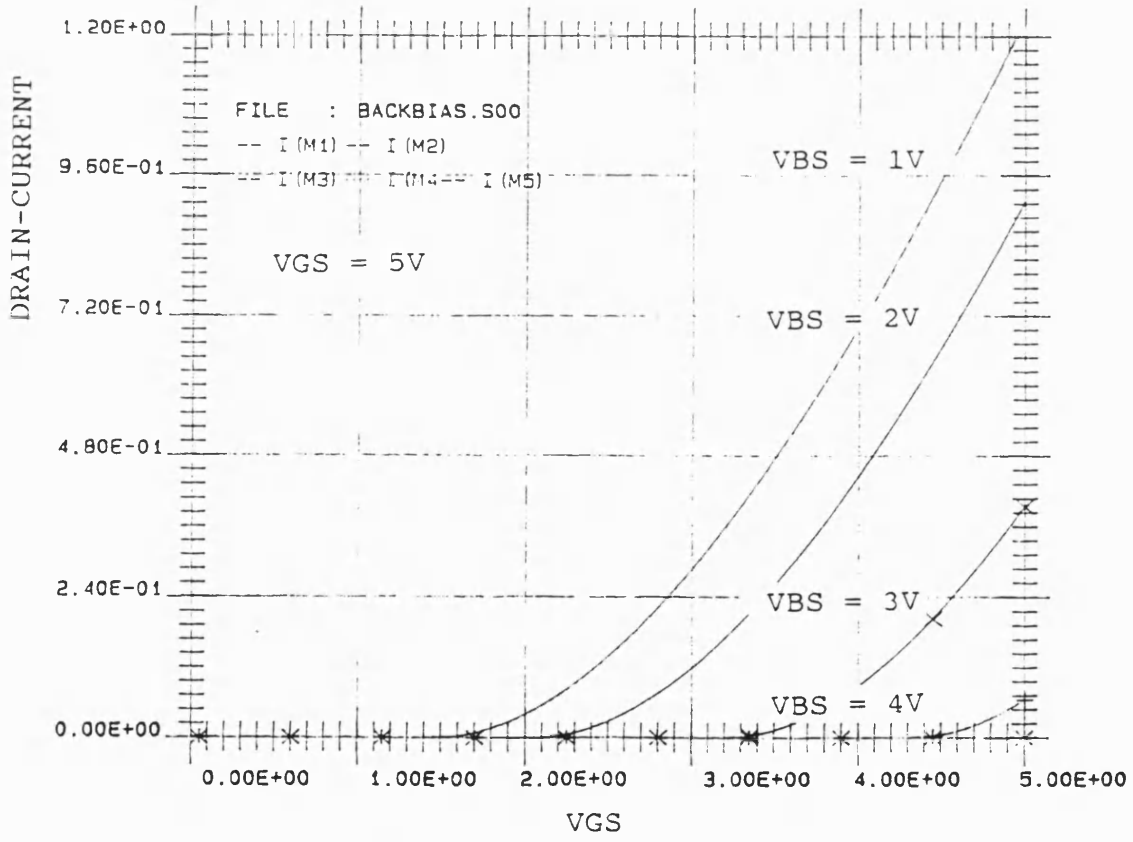

Figure 2.6 Backbias effect

2.2.3 Nonsaturation Behaviour

The nonsaturation region, otherwise called the triode or linear region, is terminated by the pinch-off effect. That means an increasing drain to source voltage with a constant gate voltage forces the channel to pinch off at a critical voltage. The electrical field intensity, when the channel starts to pinch off is called the saturation electrical field intensity E_G [9]. In [9] the saturation field is described and from [15] is given by the following expression:

$$E_G = 2 \cdot \sqrt{\frac{\Phi_S \cdot q \cdot N_B}{\varepsilon_0 \cdot \varepsilon_{Si}}} \tag{2.14}$$

In figure 2.3 the pinch off points on each curve for the two transistor types are connected with a dashed line. This line forms the pinch off parabola. Towards the zero point is the linear or nonsaturated region, and beyond the pinch off parabola is the saturated region. The transistor behaviour in the linear region will now be discussed.

The equations used in BONSAI are derived from [9]. The drain current is given by:

$$I_D = \beta \cdot \left(\left(V_{Geff} - \frac{V_{DS}}{2} + K1 \cdot \sqrt{\Phi_S + V_{SB}} \right) \cdot V_{DS} - \frac{2}{3} \cdot K1 \cdot \left((\Phi_S + V_{SB} + V_{DS})^{\frac{3}{2}} - (\Phi_S + V_{SB})^{\frac{3}{2}} \right) \right) \tag{2.15}$$

The effective gate to source voltage V_{Geff} is the gate control voltage minus the threshold voltage, ie.:

$$V_{Geff} = V_{GS} - V_T$$

Beta in equation (2.15) is the transistor specific conductance constant.

$$\beta = \frac{\beta_0}{1 + \frac{V_{DS}}{L \cdot E_C}} \tag{2.16}$$

where E_C is the critical field intensity, defined in BONSAI as:

$$E_C = 80 \cdot \frac{C_{C_{Ox}}}{B0}$$

In the model parameter set of BONSAI, beta is implemented using the parameter B0. B0 is the conductance constant independent of the transistor. Therefore beta is expressed in terms of B0 using the following relation:

$$\beta 0 = B0 \cdot \frac{W}{L} \cdot \left(\frac{298.15K}{\Delta T + T0} \right)^{1.5} \tag{2.17}$$

where: T0 is the absolute temperature of 273.15K

ΔT is the actual temperature difference to 273.15K.

The calculation of equation (2.15) for initiating a BONSAI transistor description using a simple pocket calculator is not a difficult task. Pocket calculator design can be performed with the Shichman-Hodges transistor model [16]. The drain current transistor behaviour is given by (2.18):

$$I_D = B0 \cdot \frac{W}{L} \cdot \left(V_{Geff} \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{2.18}$$

The threshold voltage implicit in V_{Geff} must obviously be calculated for the backbiased transistor. By curve fitting between the simple equation (2.18) and the computer parameter set expression (2.15) the conductance constant used in 2.18 is given by:

$$B0 = 0.75 \cdot B0_{parameterset}$$

2.2.4 Saturation Behaviour

Saturation begins beyond the channel pinch off effect with increased V_{DS}. The electrical field at the pinch off condition is given by equation (2.14). In [9] the calculation of the drain source pinch off voltage is done by an iterative method. Beyond V_{Dss}, the drain current does not increase linearly with the gate voltage. The increase is nearly a quadratic function of the gate control voltage. The channel length is decreasing within this region. This is a function of the space charge between the gate voltage controlled channel and the drain. The drain current dependence on the channel length modulation is given in [9] as:

$$I_D = \frac{I_{DS}}{1 - \frac{L_D}{L}} \tag{2.19}$$

A reasonable calculation of the drain current is presented in [17]:

$$I_D = \frac{B0}{2} \cdot \frac{W}{L} \cdot V_{Geff}^2 \tag{2.20}$$

The channel length modulation constant K2 is equivalent to the Early constant of bipolar transistors. K2 gives the slope of the output characteristic within the saturation region.

$$K2 = \sqrt{\frac{2 \cdot \varepsilon_0 \cdot \varepsilon_{Si}}{q \cdot N_B}} \tag{2.21}$$

In [9] the calculation of L_D is given as a function of the channel length modulation constant, the saturation electrical field intensity E_G and a correcting factor of L_D is given as:

$$L_D = \frac{K2}{F} \cdot \left(\sqrt{V_{DS} - V_{DSS} + \left(\frac{K2 \cdot E_G}{2F} \right)^2} - \frac{K2 \cdot E_G}{2F} \right) \tag{2.22}$$

Normally F is in the range from 1.7 to 2.2. Within the simulations in this work K2 is set to 2.

In respect to channel length modulation, equation (2.20) can be rearranged to:

$$I_D = \frac{B0}{2} \cdot \frac{W}{L} \cdot V_{Geff}^2 \cdot \left(1 + \frac{L}{L - L_D} \right) = \frac{B0}{2} \cdot \frac{W}{L} \cdot V_{Geff}^2 \cdot (1 + \alpha) \tag{2.23}$$

where: $\alpha = l \cdot V_{DS}$

l = slope of the saturation characteristic 1/V

2.3 Small Signal Transistor Modelling

Small signal parameters are defined in terms of the changes of the drain current with respect to the change of voltages at the gate, the drain to source voltage drop, and the bulk to source voltage difference. Therefore the drain current can be expressed as a function of all the applied voltages:

$$I_D = f(V_{Geff}, V_{DS}, V_{BS}) \tag{2.24}$$

The small signal parameters are :

1. the transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.25}$$

2. the channel conductance

$$g_{DS} = \frac{\partial I_D}{\partial V_{DS}} \tag{2.26}$$

3. the substrate conductance

$$g_{BS} = \frac{\partial I_D}{\partial V_{BS}} \tag{2.27}$$

Within the output characteristics of a transistor, the changes between two currents I_{D1} and I_{D2} must be taken in relation to the additional drain to source voltages V_{DS1} and V_{DS2}. Solving the differentials (2.25) to (2.27) is done using equations (2.15), (2.18), and (2.20). Table 2.1 shows the solutions.

Equation (2.24) can now be written as the total differential equation:

$$\partial i_D = g_m \cdot \partial V_{GS} + g_{DS} \cdot \partial V_{DS} + g_{BS} \cdot \partial V_{BS} \tag{2.28}$$

The voltage amplification of a transistor is defined as the ratio of output voltage to input voltage. Let us assume the drain current of a transistor is constant at each operating point, then equation (2.28) gives 0. Further more we can make an assumption that in most applications the source to bulk voltage is 0V.

Then equation (2.28) can be rewritten as:

$$\partial i_D = 0$$

$$g_{BS} \partial V_{BS} = 0 \tag{2.29}$$

$$A = \frac{\partial V_{DS}}{\partial V_{GS}} = -\frac{g_m}{g_{DS}} \tag{2.30}$$

The channel resistance is, in most switched circuits, the parameter of most interest. The channel "on" resistance is :

$$r_{on} = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{g_{DS}} \tag{2.31}$$

The small signal equivalent circuits for some applications will be presented in chapter 3 in which the simulations are described in detail.

small signal parameter	solution from equation	solved differential equation
g_m	(2.15) nsat	$B0 \cdot \frac{W}{L} \cdot V_{DS}$
g_m	(2.18) nsat	$B0 \cdot \frac{W}{L} \cdot V_{DS}$
g_m	(2.20) sat	$B0 \cdot \frac{W}{L} \cdot V_{Geff}$
g_{DS}	(2.15) nsat	$B0 \cdot \frac{W}{L}\left((V_{Geff} - V_{DS}) - K1 \cdot (\Phi + V_{SB} + V_{DS})^{\frac{1}{2}}\right)$
g_{DS}	(2.18) nsat	$B0 \cdot \frac{W}{L} \cdot (V_{Geff} - V_{DS})$
g_{DS}	(2.23) sat	$\frac{1}{2} \cdot B0 \cdot \frac{W}{L} \cdot V_{Geff}^2 \cdot 1$
g_{BS}	(2.15) nsat	$\frac{1}{2} \cdot B0 \cdot K1 \cdot V_{DS} \cdot (\Phi_S + V_{SB})^{-\frac{1}{2}}$
g_{BS}	(2.18) nsat	
g_{BS}	(2.20) sat	

Table 2.1: Summary of nonsaturation and saturation parameters

nsat : nonsaturation sat: saturation

2.4 Capacitor Models

Capacitors are one of the most critical elements in CMOS designs. They are used in A to D converters for charge sharing, in filters for frequency specification, in integrator circuits, and for offset cancellation in amplifier and comparator circuits. Therefore capacitors must be implemented carefully, the parasitic effects of stray capacitances, fringing effects, and mismatching must always be taken into account

during the design work. The following sections describe the capacitor modelling, the fringe effects and the overlap capacitance. ,

More details will be given in the chapter three.

2.4.1 BONSAI Transistor Capacitance Models

The capacitor models of BONSAI are presented in [9]. The equations used are split into two regions : nonsaturation and saturation. Within nonsaturation the capacitor equations are more complex and are given as:

$$C_{GS} = \frac{2}{3} \cdot C_{Ox} \cdot \frac{V_{Geff} \cdot \left(3V_{Geff} - 2\frac{V_{Geff} \cdot V_{DS}}{V_{DSS}} \right)}{\left(2V_{Geff} - \frac{V_{Geff} \cdot V_{DS}}{V_{DSS}} \right)^2} + C_{Ov} \tag{2.32}$$

$$C_{GD} = \frac{2}{3} \cdot C_{Ox} \cdot \left(3V_{Geff} - \frac{V_{Geff} \cdot V_{DS}}{V_{DSS}} \right) \cdot \frac{V_{Geff} - \frac{V_{Geff} \cdot V_{DS}}{V_{DSS}}}{\left(2V_{Geff} - \frac{V_{Geff} \cdot V_{DS}}{V_{DSS}} \right)^2} + C_{Ov} \tag{2.33}$$

$$C_{GB} = 0$$

$$C_{Ox} = \frac{\varepsilon_0 \cdot \varepsilon_{Ox}}{t_{Ox}} \cdot W \cdot L \tag{2.34}$$

Within the saturation region the gate to drain and gate to bulk capacitances are 0. The gate source capacitance is:

$$C_{GS} = \frac{2}{3} \cdot C_{Ox} \tag{2.35}$$

The capacitances in a switched off transistor are zero.

2.4.2 CMOS Capacitor Layout Considerations

CMOS capacitors can be designed with double poly-silicon or with metal over poly-silicon. The poly oxide thickness in double poly processes is comparable to the thickness and the quality of the gate oxide. Metal to poly-silicon capacitances use the intermediate oxide as the dielectric. The intermediate oxide thickness is about 1μm, the gate - oxide thickness is about 40 nm. Therefore double poly capacitances have a bigger unit capacitance than metal capacitances with the same size. High accuracy of capacitance value requires the elements to be manufactured as accurately as possible. In the case of capacitors, most of the critical effects derive from the manufacturing processes. There are mask misalignments, variations of the oxide thickness, and fluctuations of the permittivity. In [17] these effects are fully described. This paper points out that there is an optimum in size and geometry. This optimum for the NMOS 3.5μm silicon gate process is in the range from 50μm x 50μm up to 75μm x 75μm. Allstot and Black [18] demonstrated an improvement of 10 dB of the power supply rejection (PSR), if the capacitor array is laid out within a hard grounded p-well.

Other factors which affect the accuracy are in the matching of a capacitor array and the stray capacitances due to the different layer structures in MOS technologies. The matching properties can be handled with the design of unit element capacitors. That means there will be one capacitor designed and all the other values used within the circuitry are built with this unit element. In these designs the relative tolerance is normally the criterion. Experience in these designs show suitable unit capacitors laid out are of the lowest capacitance value used in the circuit (in A to D converters the

minimum capacitance value is normally the capacitance corresponding to the LSB). Due to edge effects, see [18], the lay-out of a unit capacitor should be octagonal with 45° edges. This design basically has two advantages:

1. enhanced stability against underetching, which increases accuracy

2. advantages due to high density packaging, which means less effects from fluctuations in oxide thickness and permittivity.

There are still other effects in MOS capacitors that contribute to the accuracy. In [19] two effects are described :

1. parasitic capacitor effect

2. backbias effect

Parasitic capacitance occurs at the edges of the capacitor adding to the bottom plate to bulk capacitance. The edge effects or fringing effects contribute to about 10% of the designed capacitor value. These parasitic effects, the interconnect lines and the plate capacitors, will be discussed in the next section 2.5.

The backbias effect depends on the substrate voltage. The capacitance C_{Si} (substrate) to SiO_2 (oxide) is voltage dependent. The effect of this voltage dependence can be studied with the help of the C-V curve (see Appendix I).

2.5 Fringing Effects

The capacitance of interconnect lines and of capacitor structures is affected by homogeneous and inhomogeneous electrical fields. The increase of the capacitor value because of the inhomogeneous electrical field is well known as the fringe effect and was studied [20-25] to improve the computation of the capacitance of interconnect lines of integrated circuits. The influence of fringing on the capacitor value increases with a decrease in the device geometry. It is important, however, to examine the influence of this effect for interconnections and for capacitor structures. This work was done as a student project, at Plymouth Polytechnic under supervision of the author [25], which shows the various theoretical models, improved measurement procedures, the results and the auxiliary FORTRAN Programs to compute the correction terms.

2.6 Propagation Delays of Interconnect Lines

Propagation delays limit the speed of integrated circuits. The effects are comparable to the behaviour of other high frequency interconnections, especially well known in the field of microwave engineering.

In [26] descriptions are given of cut off frequencies and measured propagation delays using the method of unity elements. In [26] the author uses buffer elements within long interconnect lines (bigger than a few hundred micrometres). This is a useful idea for the digital field. Propagation delays of about 40ps/μm are achievable. In [27] the behaviour of interconnections are examined using the finite element method. The authors examine four line shapes, and study the reflections on the edges of bends with and without 45° chamfering. The 45° angle is preferable because there is less distortion in the electric fields compared to the unchamfered bends.

2.7 Overlap Capacitances

The overlap capacitances are parasitics arising from the gate to source and gate to drain area overlap. Overlap capacitances in the area of self aligned CMOS processes contribute to parasitic effects like the clock feed through problem. In [28] a simple formula to calculate the overlap capacitance is discussed. Note that the table 1 in [28] shows overlap capacitances as unit capacitances, an overlap capacitance of 0.5 $fF/\mu m^2$. In [29] the overlap capacitances were measured between 0.2 $fF/\mu m^2$ (silicon gate) and 2.2$fF/\mu m^2$ (Al -gate). Therefore the calculation of the overlap capacitance of a real device is given in BONSAI as:

$$C_{Ov} = 0.5\frac{fF}{\mu m^2} \cdot (W_{Geff} \cdot \Delta L) \tag{2.36}$$

$$C_{Ov} = (\Delta L + F_L) \cdot W \cdot C_{Gox}$$

where: ΔL : overlap distance

F_L : length fringing factor

W_{eff}: width of the gate

C_{Gox} : gate oxide capacitance

C_{Ov} : overlap capacitance

$$C_{Diff} = C_{Ov} \cdot \left(\frac{\Phi_D}{\Phi_D + V_S}\right)^{Cexp} \tag{2.37}$$

where: Φ_D : diffusion potential

V_S : source voltage

Cexp : exponent for the inversion capacitance

2.8 Noise

2.8.1 Introduction to Noise Theory

Noise, an ever present problem in all fields of electrical engineering, has been known of since the first observations of temperature dependent movements of small particles by Anton van Leeuwenhoek about 1715 [30] and was further described by Brown in 1827. Noise within this work will be confined to the field of internally generated noise of resistors and MOS structures. Basic noise theory is described in many publications [31-37].

The physical description of noise divides this section into:

- thermal noise
- shot noise
- generation and recombination noise
- flicker noise

From studies of Brownian motion, thermal noise was predicted. It was first observed by J.B.Johnson of Bell Telephone laboratories in 1927, and a theoretical analysis was provided by H.Nyquist in 1928. Because of their work thermal noise is called Johnson or Nyquist noise [36]. The thermal noise [32,33,35,36] is the energy "floor", that means a constant noise level over a wide frequency range. Shot noise [35] is produced within p-n junctions and is not relevant in the field of MOS noise, because the current flow is drift of carriers through ohmic conduction and not by carriers crossing a potential barrier. Generation and recombination noise is produced by the statistical variation of the time constants of free electric charge carriers [31]. Flicker noise [34-36] shows an indirect relationship between the frequency and the resulting equivalent input noise voltage. Flicker noise is only relevant at low frequencies.

2.8.2 Noise of Resistors

The power consumption in resistors generates thermal energy. This energy can be described as a random movement of particles. The auto-correlation-function (ACF) of a noise emitting resistor is given by eqn.(2.38) [37].

$$\rho(\tau) = 2 \cdot R \cdot (\pi \cdot k \cdot T)^2 \cdot \left(\left(\frac{h}{2 \cdot \pi^2 \cdot k \cdot T \cdot \frac{1}{f}} \right)^2 - \frac{1}{\sinh^2\left(\frac{2 \cdot \pi^2 \cdot k \cdot T \cdot \frac{1}{f}}{h} \right)} \right) \tag{2.38}$$

This equation shows no dependence on supply voltage. The Fourier transformation of eqn.(2.38) gives the spectrum of the noise power density $\omega(f)$ as:

$$\omega(f) = 4 \cdot R \cdot k \cdot T \quad + \quad \frac{h \cdot f}{k \cdot T \cdot \left(e^{\frac{h \cdot f}{k \cdot T}} - 1 \right)} \tag{2.39}$$

where: h : the quantisized Planck constant

k : the Boltzmann constant

$h = 6.60 \cdot 10^{-34} Ws^2$

$k = 1.38 \cdot 10^{-23} \frac{Ws}{K}$

The explicit computation of the right term in eqn. (2.39) within the frequency range up to 1 GHz is much less than 1. Therefore eqn. (2.39) can be simplified, the resulting new equation gives the Nyquist law:

$$\omega(f) \cdot \Delta f = 4 \cdot k \cdot T \cdot R \cdot \Delta f = \overline{v}^2 \tag{2.40}$$

The standard room temperature of 20°C gives the standardisation of eqn. (2.40):

$$\bar{v}_{20^\circ} = 40 \cdot \sqrt{R \cdot \Delta f \cdot 10^{-23}} \tag{2.41}$$

With the help of eqn. (2.40 and 2.41) the noise voltage of a noisy resistance with the frequency as an independent variable can be drawn as shown in figure 2.9 (R is the ideal resistance). Figure 2.10 shows the noise current $\bar{i}$ as a function of the resistance and the DC - current of the resistance.

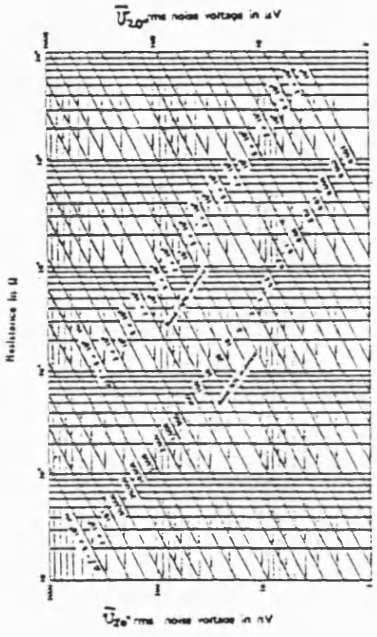

Figure 2.9

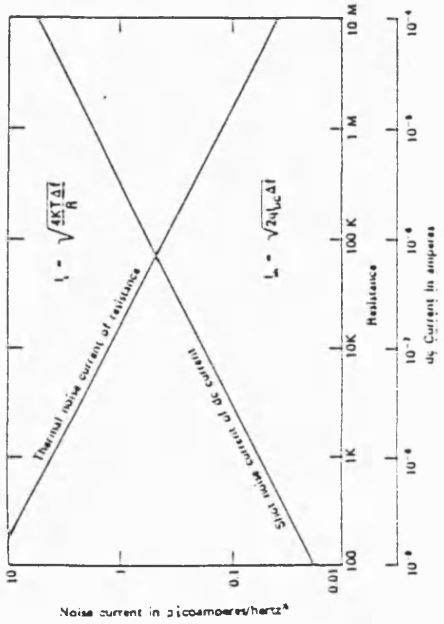

Figure 2.10

2.8.3 Noise in MOS Structures

The MOS transistor can be simplified to a voltage controlled resistor. Because of this nature, we expect the noise characteristic shown in eqn. (2.40) and a low frequency component, which gives a linear increase of the noise power by decreasing of the frequency range. This characteristic is produced by trapping of channel charges. Decreasing the frequency below about the 1Hz limit results in a more constant noise

power. This effect is based on centers of generation and recombinations zones, especially at the Si-SiO_2 interface. Because of the very low frequency range, this kind of noise figure is very difficult to examine.

2.8.3.1 Noise of Generation and Recombination

There are two methods of analysing the generation and the flicker recombination noise of free charges [31]. Appendix I shows the computation of the CV - characteristic useful for the Sze procedures. The CV analysis is easy to use to detect and evaluate the time constants of the charge carriers in MOS structures. Sze presents two methods using the CV-characteristics:

Method 1:
Capacitance Method:
Measurement of ratio of MIS capacitance of oxide capacitance

Method 2:
Conductivity method:
Measurement of the conductivity of MIS and oxide capacitances

Method 1: Capacitance Method

There are 3 different analyses to measure noise effects:

1.) The differential procedure

Proposed by Terman [38], analysis of the high frequency CV-curve with the slope descending from the accumulation region of the MOS structure towards weak

inversion (here it is a flat minimum) and the stable CV-region, - perhaps a little above the minimum at weak inversion - over the strong inversion range. This procedure extracts the effect of the charges in the surface states.

2.) The integration procedure

Berglund [39] proposed that the semiconductor surface potential can be determined directly from the low-frequency differential capacitance measurement. Integration of this curve gives the surface potential. This procedure is only valid within equilibrium of the surface states at any time. Therefore the CV-characterisation frequency must be low.

3.) The temperature procedure

Gray and Brown [40] offered this method to separate the effects of space charges in the insulator and the surface states of the surface potential. Plotting the CV-curve at different temperatures, a shift of the slopes towards strong inversion was detected with increasing temperature. The requirement of this procedure is the flat band voltage condition. During the flat band condition there is no accumulation of n- or p- type charges at the interfaces and hence no band bending. The changes in capacitance need the adjustment of the bias voltage to hold the MOS structure in flat band condition during measurement versus temperature. Plotting the surface charge versus surface potential gives the number of surface states.

Method 2: Conductivity Method

Extracting the capacitance of surface states from the measured capacitances of oxide and free space charges with the capacitance method is difficult, because of the

small changes in capacitance. The conductivity method to extract the conductance of the free space charges is more accurate. In the case of equilibrium between the density of surface states and charges in SiO_2 the conductivity method is very precise. The conductivity of a capacitance over the range of the bias voltage during a CV-plot, shows a difference between the maximum and the floor level of more than an order of magnitude.

The advantage of both methods is in the possibility to measure the capacitance and conductivity in parallel with the same equipment. Sze gives a detailed description of this method and how to extract the time constants for the generation and recombination (g-r) processes.

The time constants of the g-r processes are in the range below of 10 Hz. The flicker noise of semiconductors is dominant above the g-r noise level.

2.8.3.2 Noise in MOS Transistors

1.) thermal noise

The origin of thermal noise is the finite channel resistance of a transistor. The channel noise of a MOS FET can be related very closely to the noise generated in resistors. Hence the noise induced by the transistor channel can be described as:

$$\frac{\overline{v_{nT}^2}}{\Delta f} = \frac{4 \cdot k \cdot T}{\frac{2}{3} g_m} \tag{2.42}$$

Eqn. 2.42 can be described more accurately by taking the desired bandwidth into account. Therefore eqn.(2.42) can be rearranged to:

$$\overline{v}_{nT}^2 = \int_{f1}^{f2} \frac{\overline{v}_{nT}^2}{\Delta f} df = \frac{4 \cdot k \cdot T}{\frac{2}{3} g_m} \cdot (f2 - f1) \tag{2.43}$$

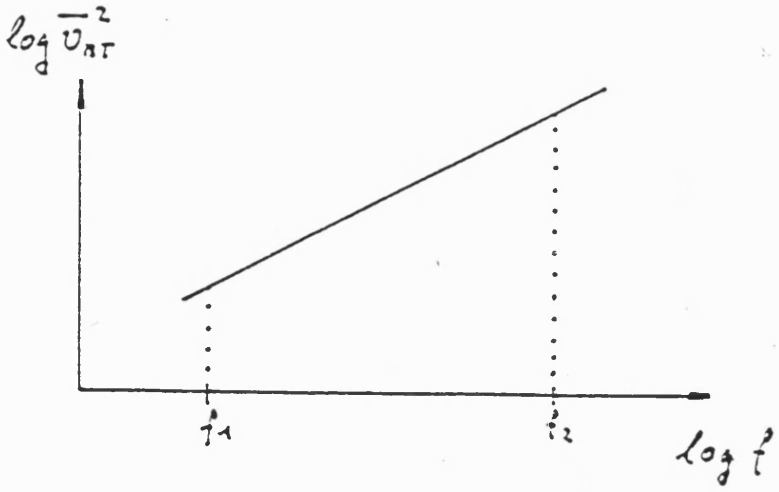

Figure 2.11 Noise power versus frequency

Figure 2.11 shows the graph of eqn.(2.43). Increasing the bandwidth Δf is proportional to the increase of the equivalent noise voltage. This feature affects the design of low noise structures dramatically. In chapter 3.3, a low noise operational amplifier design approach using eqn.(2.43) will be presented.

The thermal noise description of a MOS transistor is based on the equivalent circuit of the transistor channel as a RC - network built of the channel conductance and the junction capacitance.

$\overline{v}_{nT}^2/\Delta f$ is the input noise power of this circuit. R is the resistance of the channel and C is the junction capacitance. The voltage drop over the junction is v_0. The following procedure illustrates that the noise level for high frequencies can be expressed as a constant dependent only on the capacitance value of the device.

$$\frac{\overline{v_{0n}^2}}{\Delta f} = \frac{\overline{v_n^2}}{\Delta f} \cdot \left| \frac{G}{G + j \cdot \omega \cdot C} \right|^2 \tag{2.44}$$

$$\overline{v_{0n}^2} = \int_0^\infty \frac{\overline{v_n^2}}{\Delta f} \cdot \frac{G^2}{G^2 + (\omega \cdot C)^2 + j \cdot 2 \cdot G \cdot \omega \cdot C} d\frac{\omega}{2 \cdot \pi}$$

$$\overline{v_{0n}^2} = \frac{4 \cdot k \cdot T \cdot R \cdot G^2}{2 \cdot \pi} \cdot \int_0^\infty \frac{1}{G^2 + (\omega \cdot C)^2} d\omega$$

$$\overline{v_{0n}^2} = \frac{4 \cdot k \cdot T}{2 \cdot \pi \cdot C} \cdot a \quad \tan \frac{C \cdot \omega}{G} \Big|_0^\infty$$

$$\overline{v_{0n}^2} = \frac{4 \cdot k \cdot T}{2 \cdot \pi \cdot C} \cdot \left(\frac{\pi}{2} - 0 \right) = \frac{k \cdot T}{C} \tag{2.45}$$

2.8.4 Flicker Noise in MOS FET's

The origin of flicker noise is in the fluctuations of channel charge due to trapping by surface states. Flicker noise decreases down to the constant thermal noise floor with an increase of the frequency.

Flicker noise has a significant effect in MOS designs. Hence low noise designs should be first order optimized to the frequency dependent flicker noise. McCreary gives the relation between the equivalent flicker noise voltage $\overline{v_{nF}^2}$ and the frequency f [41] as:

$$\frac{\overline{v_{nF}^2}}{\Delta f} = \frac{K_F \cdot I_D}{C_{Ox} \cdot L^2 \cdot g_m} \cdot \frac{1}{f} \tag{2.46}$$

Rearrangement of eqn.(2.46) with g_m from table 2.1 gives eqn.(2.47).

$$\frac{\overline{v_{nF}^2}}{\Delta f} = \frac{K_F}{2 \cdot \mu \cdot C_{Ox}^2} \cdot \frac{1}{W \cdot L} \cdot \frac{1}{f} \tag{2.47}$$

In chapter 3.3 we will see that the term $1/W \cdot L$ in eqn.(2.47) requires a large active area to decrease the noise spectrum.

K_F is called the flicker noise coefficient. The following example gives an idea of the order of magnitude of the equivalent noise voltage density:

Pick: $W/L = 10$; $t_{Ox} = 70nm$; $f = 1KHz$

Then:

$$\frac{\overline{v_{nF}^2}}{\Delta f} = 95 \frac{nV}{\sqrt{Hz}} \tag{2.48}$$

The proportional dependence of $1/f$ and $\overline{v_{nF}^2}/\Delta f$ results in a 10 dB decrease per each decade. McCreary [41] gives the following values for K_F (t_{Ox}=100 nm):

$K_F = 3.4 \cdot 10^{-28} AF$ without implantation

$K_F = 4.5 \cdot 10^{-28} AF$ enhancement implantation

$K_F = 6.5 \cdot 10^{-28} AF$ depletion implantation

The p-channel and n-channel transistors show the following dependence of the noise coefficients:

$$\frac{K_{Fp}}{K_{Fn}} = \frac{\mu_p}{\mu_n} \tag{2.49}$$

μ_p, μ_n are the mobilities of the charge carriers in a p-channel and a n-channel device respectively. Based on eqn.(2.46), the limit of Δf to zero rearranges eqn.(2.46) to give:

$$\lim_{f \to 0} \frac{\overline{v}_{nF}^2}{\Delta f} = \lim_{f \to 0} \frac{K_F \cdot I_D}{C_{Ox} \cdot L^2 \cdot g_m^2} \cdot \frac{1}{f} = V_{Off,FN} \qquad (2.50)$$

The noise voltage at DC can be modelled as an additional offset voltage. Depletion transistors have a lower flicker noise than enhancement transistors because of the buried channel layer in the depletion technique. Hence low noise component designs should be done with depletion input stages, if possible. The influence of surface states and traps is minimized because of the channel distance from the Si - SiO_2 interface in depletion transistors.

The following plots (fig. 2.10, 2.11) show the typical noise behaviour of MOS transistors in terms of the noise equivalent resistance R_N versus the frequency and versus the drain current, respectively [31].

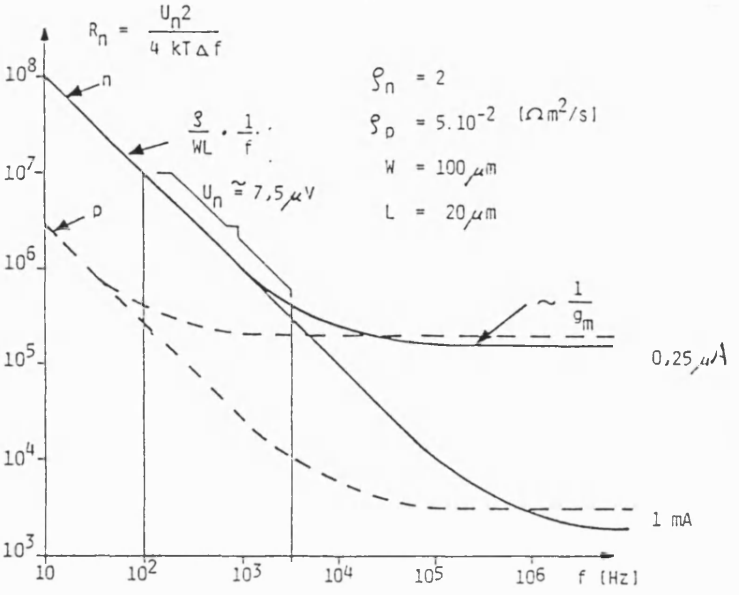

Figure 2.10

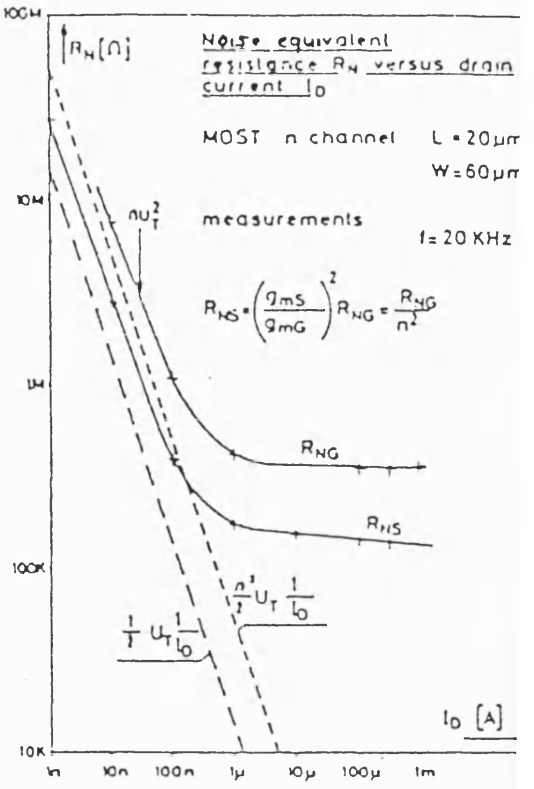

Figure 2.11

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C H A P T E R 3

ANALOGUE BUILDING BLOCKS

Building blocks are by definition functional blocks to be used in integrated circuit designs. The advantage of defining analogue circuits in terms of building blocks, is that a cell may be standardized and defined in terms of its interface description and terminal locations. The development of VLSI analogue circuits can be broken down into building blocks. On completion, the blocks are assembled to form the functional circuit. Four different building blocks will be developed as standard components within this work:

- Transfer-gate
- Comparator
- Chopper stabilized OTA
- Chopper fully differential OTA

3.1 Transfer-Gate

Transfer-gates are in common use as switches in analogue integrated circuits. In CMOS circuits, paired transfer-gates, i.e. p-channel and n-channel transistors connected in parallel, are most often used, to minimize parasitic effects. These transfer-gates are clock controlled. Three factors must be discussed in switched circuits:

1. clock feed through
2. limited on resistance
3. noise

These factors lead to a decrease in the accuracy and speed of the transfer-gate.

3.1.1 Clock Feed Through

Clock feed through is charge injection arising from the clock edge. Figure 3.1.1 shows a symmetric transfer-gate including the internal capacitances. CMOS designs use p- and n-channel transistors as parallel elements. They are clocked symmetrically as shown in figure 3.1.2. The clock lines are connected to the transistor gates of the transfer-gates. Due to the capacitance of the transistor, the clock edge induces a charge through this capacitance into the capacitance of the signal line and connected elements. The first publication using the term clock feed through was by Stafford et al, [1]. In [1] to [7], clock feed through cancelling techniques are described. Most popular in NMOS designs are charge cancelling devices. Charge cancelling devices are transistors of the same conductivity type, connected as dummy elements at the source and drain side of the transfer-gate which are clocked inversely (fig. 3.1.2).

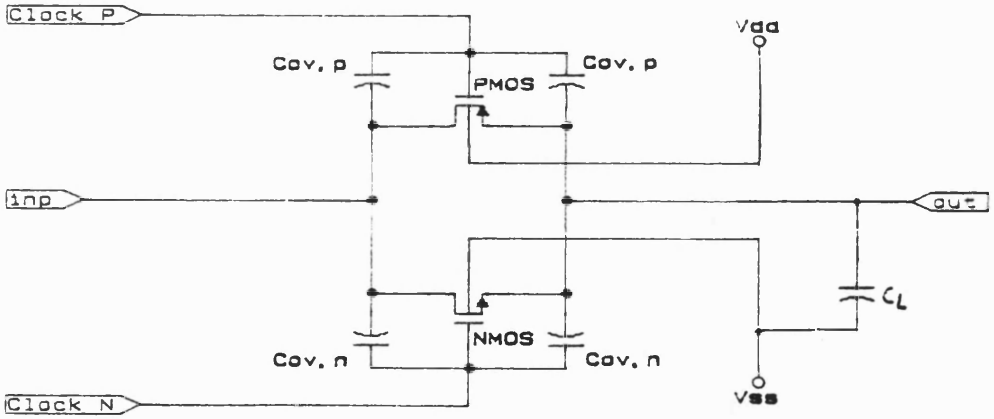

Figure 3.1.1 Symmetric Transfer-Gate

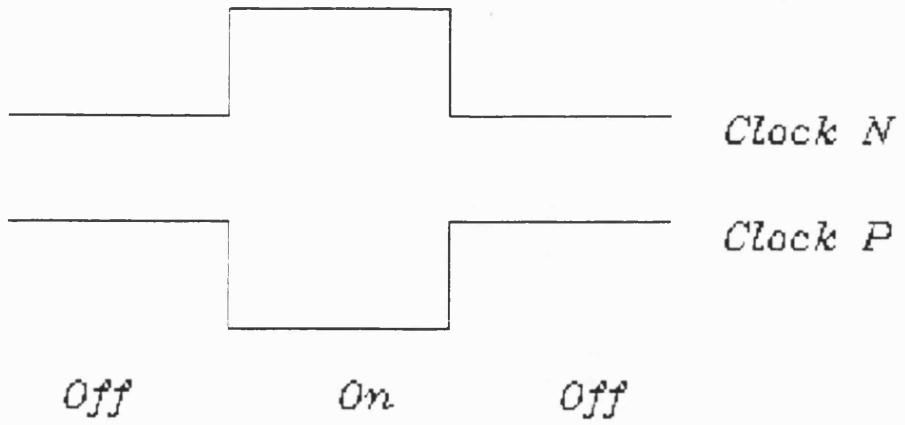

Figure 3.1.2 Clock Scheme of a Transfer-Gate

3.1.1.1 Simplification

Let us assume an equivalent charge flow per unit time for charging and discharging a load capacitance, then ideally all the charges flowing through the p-channel transistor will be compensated by the n-channel transistor. In reality, the clock slopes are not exactly mirror images, and so their voltage slopes are not completely matched. Therefore the clock feed through is the difference in charge resulting from the equation system (3.1.1) and (3.1.2). The simplification in (3.1.3) and (3.1.4) is valid if the clock slopes are sufficiently short in respect to the switch "on" time. The gate to substrate capacitance can be neglected in a first order calculation, if the signal is near the midrail voltage. In this case the substrate biasing of the p-channel and the n-channel transistors are nearly balanced. The major effect of parasitic capacitance comes from the overlap capacitance.

The clock feed-through can be calculated using the simplified model shown in figure 3.1.1. The charge induced in a load capacitance C_L is given by:

$$dq_p = \frac{C_L \cdot C_{ovp}}{C_L + C_{ovp}} \cdot dV_{clockp} \qquad (3.1.1)$$

$$dq_n = \frac{C_L \cdot C_{ovn}}{C_L + C_{ovn}} \cdot dV_{clockn} \qquad (3.1.2)$$

where: q_p : charge through p-channel transistor

q_n : charge through n-channel transistor

C_L : load capacitance

C_{ovp} : overlap capacitance p-channel transistor

C_{ovn} : overlap capacitance n-channel transistor

V_{clockp} : clock voltage at the gate of the p-channel transistor

V_{clockn} : clock voltage at the gate of the n-channel transistor

The index p or n indicates the conductance type of the transistor. Equations (3.1.1) and (3.1.2) can be simplified when the clock voltage slope is nearly constant within the time period.

The clock feed through charge can therefore be written as the difference of the charges flowing through both transistors into the load capacitance.

$$dq_{ft} = dq_p - dq_n \qquad (3.1.3)$$

where : q_{ft} = clock feed through charge

If $C_L >> C_{ov\,n,p}$ then:

$$dq_{ft} = C_{ovp} \cdot dV_{clockp} - C_{ovn} \cdot dV_{clockn} \qquad (3.1.4)$$

To simplify further, assume that the charges flowing through each transistor are equal. Therefore the clock feed through charge can be rearranged to:

$$\Delta q_{ft} = \frac{\Delta C_{ov}}{C_L} \cdot \Delta q_{p,n} \tag{3.1.5}$$

The voltage drop due to the clock feed through charge on the load capacitance can be written by:

$$V_{CLft} = \frac{q_{ft}}{C_L} \tag{3.1.6}$$

Note, that C_L includes the interconnect capacitance and the active element capacitances.

3.1.1.2 Improved Accuracy

The characteristics of the switch transistors will now be taken into account. In [6] a good introduction to the problem of the clock feed-through induced in transfer-gates is presented. The equations 3.1.7 and 3.1.8 describe the dependence of the clock feed through on the slope of the gate voltage. Figure 3.1.3 and 3.1.4 show the equivalent circuits for the "on" and "off" states, respectively.

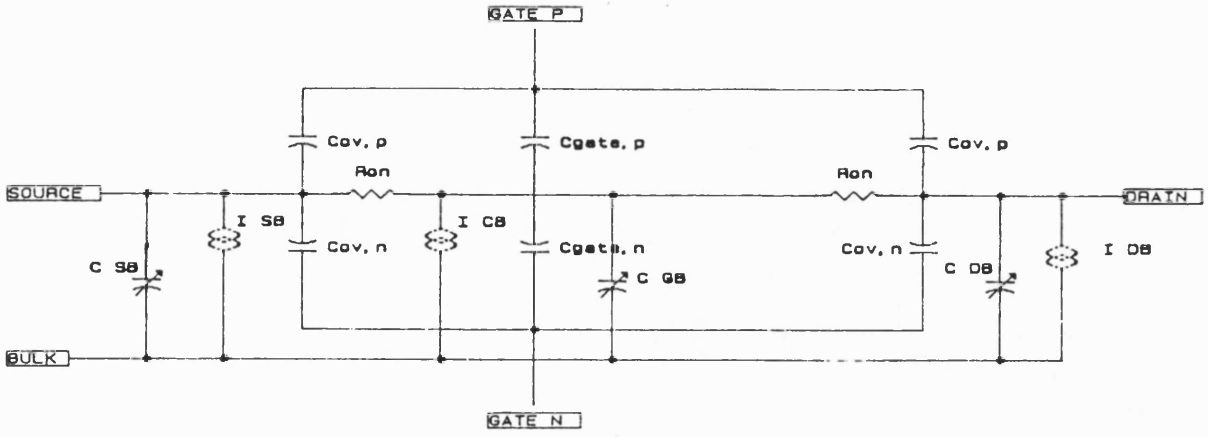

Figure 3.1.3 Transfer-gate "on-state"

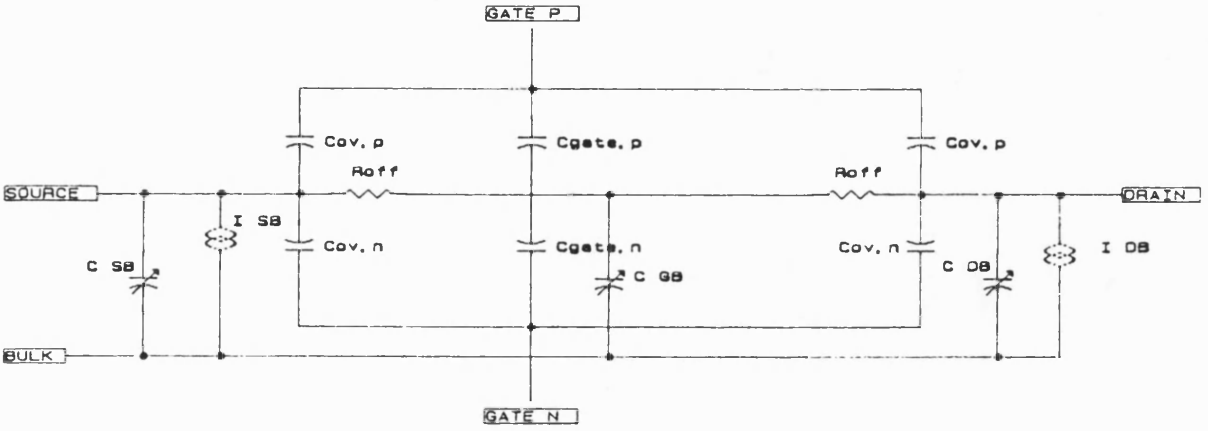

Figure 3.1.4 Transfer-gate "off-state"

The substrate bias controls the voltage dependent bulk capacitances of the source and the drain region. These capacitances are labelled with an arrow through C_{SB} and C_{DB}. During switch on, the transfer-gate transistors can operate in saturation and/or nonsaturation region. In the "off" state, the transistor channel is switched off and the transistor is in accumulation mode. The overall clock feed-through charge during rising or falling clock slope can be approximated as:

$$q_{ft} = 2 \cdot C_{ov} \cdot V_{DD} + \int_{V_{GS}}^{V_{DD}} C_{ox} \cdot dV \tag{3.1.7}$$

$$q_{ft} = 2 \cdot C_{ov} \cdot V_{DD} + C_{ox}(V_{DD} - V_{GS}) \tag{3.1.8}$$

Each transistor in a transfer-gate has nearly the same oxide capacitance in the region of the midpoint voltage. Calculation of the clock feed-through voltage over the load capacitance as a function of the clock slope delay is given as:

$$q_{ft} = \int_{t=0}^{t=tl} I_{ovp} \cdot dt - \int_{t=0+td}^{t=tl+td} I_{ovn} \cdot dt \tag{3.1.9}$$

$$q_{ft} = C_{Ovp} \cdot V_{GSp}(t) - C_{Ovn} \cdot V_{GSn}(t + td) \tag{3.1.10}$$

where: I_{ovp}: current through the overlap capacitance of the n-channel transistor

I_{ovn}: current through the overlap capacitance of the p-channel transistor

Equation (3.1.10) can be rearranged in terms of the load capacitance connected to the sources.

$$q_{ft} = \frac{C_{Ovp} \cdot C_L}{C_{Ovp} + C_L} \cdot V_{GSpVss}(t) - \frac{C_{Ovn} \cdot C_L}{C_{Ovn} + C_L} \cdot V_{GSnVss}(t + td) \tag{3.1.11}$$

$$V_{CLft} = \left(\frac{C_{Ovp}}{C_{Ovp} + C_L} \cdot V_{GSpVss}(t) \right) - \left(\frac{C_{Ovn}}{C_{Ovn} + C_L} \cdot V_{GSnVss}(t + td) \right) \tag{3.1.12}$$

where: V_{GSn}: gate to source voltage of the n-channel transistor

V_{GSp}: gate to source voltage of the p-channel transistor

If $C_L \gg C_{Ov}$ *then*:

$$V_{CLft} = \frac{C_{Ovp} \cdot V_P}{C_L} - \frac{C_{Ovn} \cdot V_n}{C_L} \tag{3.1.13}$$

Equation (3.1.13) can be interpreted as a voltage difference of the remaining clock feed through error voltage. Taking $V_p = V_n = V$, equation (3.1.13) can be simplified to:

$$V_{CLft} = \frac{C_{Ovp} - C_{Ovn}}{C_L} \cdot V \tag{3.1.14}$$

The voltage dependence on the transistor capacitances are described in Appendix I. In this approach the capacitance C_{Ox} must be split into C_{GS} and C_{GD}. This description necessitates the integral of eqn. 3.1.7 and 3.1.8 to be calculated numerically. In BONSAI the clock feed-through is simulated without considering the weak inversion transition. In the case of a symmetric transfer-gate the equation (3.1.9) must incorporate time dependences as well. The two clock slopes are not matched in phase because the clock generator produces a timing delay between the two clocks. The other factors that contribute to more complications in solving the problem are differences in the threshold voltage, differences in the back biasing, and differences in the channel conductivity because of different gate areas. Symmetrically designed transfer-gates show the least influence of clock feed through, because the voltage dependent differences are minimized.

Sheu and Hu postulated another theory in the understanding of the clock feed through problem [8]. The authors consider mobile charges within the channel beneath the overlap feed through. They showed that these mobile charges lose their influence when the switch is set in the off state very slowly. This can be critical in respect to the time scheme (fig. 3.1.2), if the clock drivers are designed for high speed applications, but this idea seems to be applicable for low frequency designs.

3.1.2 The on - Resistance of a Transfer-Gate

The on - resistance of a transfer-gate contributes directly to the propagation delay time and results in an additional pole in the transfer function.

The on - resistance of a transfer-gate is the parallel resistance of the p- and n-channel transistors. Transfer-gates normally operate in the linear region within strong inversion. Therefore the source to drain current and the on resistance can be calculated as:

$$I_D = B_0 \cdot \frac{W}{L} \cdot \left(V_{Geff} V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{3.1.15}$$

$$r_{on} = \left(B_0 \cdot \frac{W}{L} \cdot \left(V_{Geff} - \frac{V_{DS}}{2} \right) \right)^{-1} \tag{3.1.16}$$

The symmetric transfer-gate on resistance can be easily calculated according to equation (3.1.16) as:

$$R_{on} = \frac{r_{onp} \cdot r_{onn}}{r_{onp} + r_{onn}} \tag{3.1.17}$$

The design of CMOS transfer-gates must take the conductivity differences of the two channel types into account. Therefore the limiting criterion is always the worse transistor type. In p-well processes this is the p-channel transistor.

3.1.3 Noise of Transfer-Gates

Most of the noise in transfer-gates is induced by the thermal activity of charge carriers in the channel. The equivalent noise voltage $\overline{v^2}$ must be expanded in switched capacitor (SC) circuits to include the time constant composed of the on resistance of the transfer-gate and the load capacitance [9]. Hence the equivalent noise voltage can be written as:

$$\overline{v^2} = \frac{k \cdot T}{C} \cdot (1 - e^{-2 \cdot t/R \cdot C}) \tag{3.1.18}$$

For steady state the last equation can be simplified to:

$$\overline{v^2} = \frac{k \cdot T}{C} \tag{3.1.19}$$

3.2 Comparators

To interface the analogue part of a circuit with the digital part, a component that achieves a direct analogue voltage to digital level transformation within the specified accuracy is required. This operation requires an analogue reference voltage that acts as a threshold. In A to D converters this process must carried out as often as the length of the desired digital word. The overall accuracy of the A to D conversion process is directly dependent on the accuracy of the comparator circuit. Hence a comparator should be developed that fulfils both accuracy and speed considerations of A to D converters up to the current state of the art, with resolution of 12 to 16 bits using a clock rate of up to 5 MHz. This section presents two possible comparator circuits: a time continuous and a time discrete device.

3.2.1 Time Continuous Comparators

Time continous comparators are based on operational amplifiers. Mostly these designs are based on two stage opamps as they require gain of about 80 to 100dB. To increase the speed of the device, the frequency compensation normally used to stabilize the amplifier at unity gain (0 dB) is neglected or else the opamp design is improved with an internal switch in order to operate with the frequency compensation during unity gain. The common mode range, as well as the power supply rejection are parameters of interest. Operational amplifiers used for comparators are sometimes optimized with respect to noise. One method to minimize the 1/f noise will now be presented. Two stage amplifiers have an input stage gain between 10 and 100. Therefore the noise optimization can be done just for the input stage. As shown in chapter 2.8.3.2, the noise figure is split into a low frequency dependent term

(proportional to 1/f) and a temperature dependent term (proportional to kT/C). Figure 3.2.1 shows a transistor with a passive resistive load, figure 3.2.2 shows a transistor with an active load transistor.

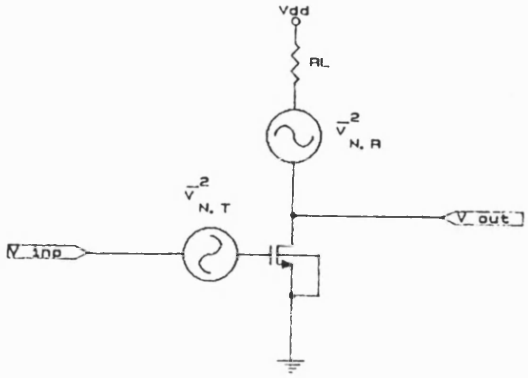

Figure 3.2.1 Noise of a transistor with a passive load

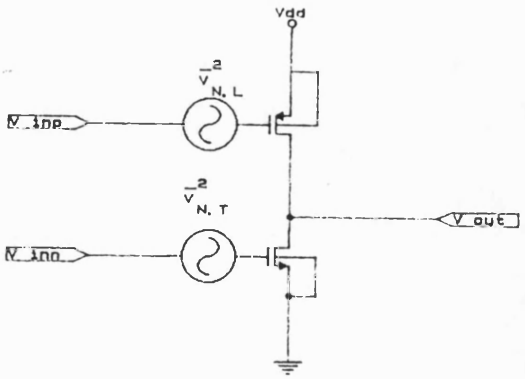

Figure 3.2.2 Noise of a transistor with an active load

Calculation of the noise is simplified by using an auxiliary noise source connected to the input of the active transistor [10,11]. This auxiliary source is called the equivalent input noise voltage. Referring to figure 3.2.1, the equivalent input noise voltage is given by :

$$V_N^2 = V_{NT}^2 + \frac{V_{NR}^2}{(g_{m,T} \cdot R_L)^2} \qquad (3.2.1)$$

where:

V_N^2 *is the equivalent noise voltage*

V_{NT}^2 *is the noise induced by the transistor*

V_{NR}^2 *is the noise induced by the resistor*

Regarding figure 3.2.2, the equivalent input noise voltage is given as:

$$V_N^2 = V_{NT}^2 + \frac{g_{m,L}^2}{g_{m,T}^2} \cdot V_{NL}^2 \qquad (3.2.2)$$

where:

$g_{m,L}$ *is the transconductance of the load transistor*

$g_{m,T}$ *is the transconductance of the input transistor*

V_{NL}^2 *is the noise induced by the load transistor*

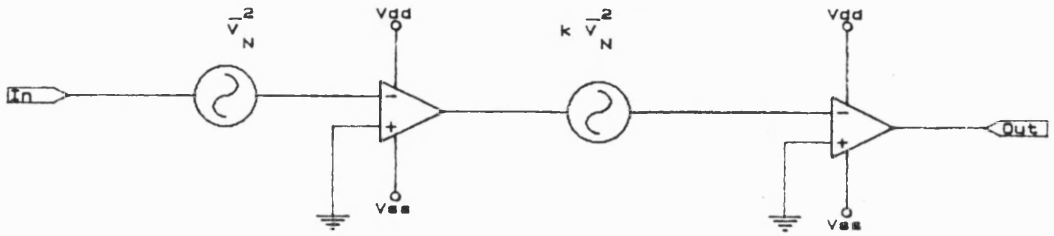

Figure 3.2.3 Noise figure in a two stage operational amplifier

Figure 3.2.3 shows a simplified equivalent circuit of a two stage operational amplifier. The factor k is the noise gain factor. Referring to figure 3.2.3, the equivalent input noise voltage is given as:

$$V_N^2 = V_{N0}^2 \cdot \left(1 + \frac{k^2}{g_m / g_{DS,1}^2}\right) \qquad (3.2.3)$$

V_{N0}^2 *is the equivalent noise of one stage*

3.2.2 Noise Optimization of a Differential Input Stage

Following Klein [12], a design procedure will be described. The 1/f noise figure of the operational input stage, if both branches have the same transistor geometries, is given by:

$$V_N = F_i \cdot \frac{I_D^{1/8}}{(W^2 \cdot L)^{1/4}} \qquad 1/f - noise \qquad (3.2.4)$$

$$V_N = \frac{k_i}{\sqrt{g_{m,i}}} \qquad thermal - noise \qquad (3.2.5)$$

where:

i is N for NMOS or P for PMOS

F_i and k_i are process and frequency dependent constants. From experimental analysis:

$$\frac{F_N}{F_P} \approx 1.3$$

$$\frac{K_N}{K_P} \approx 1.7$$

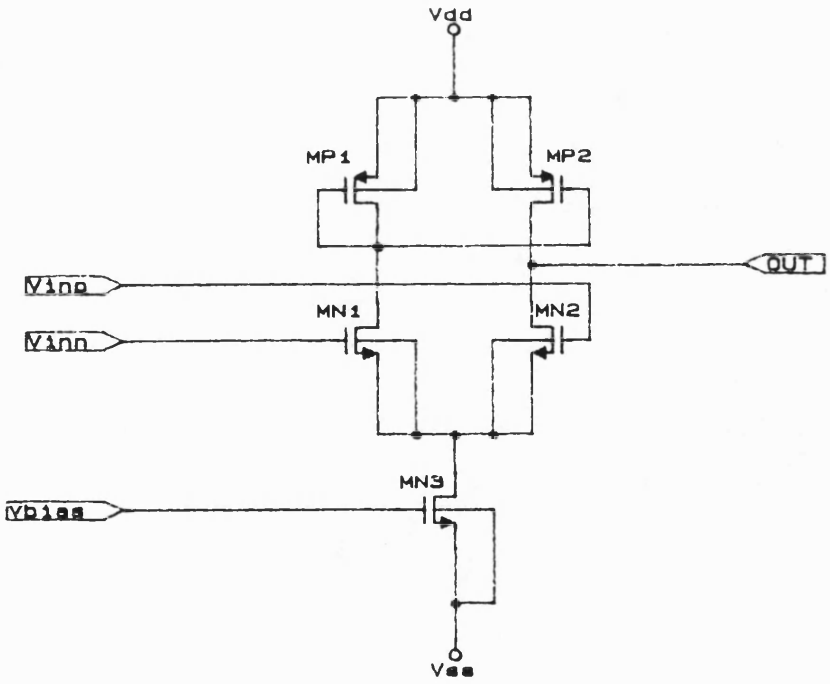

Figure 3.2.4 Differential input stage of a two stage OPAMP

Figure 3.2.4 shows the differential input stage to be optimized with respect to noise performance. The differential stage shows uncorrelated noise behaviour in both branches. The circuit can basically be explained as an adder that consists of two source followers. Hence a factor of 2 must be taken into account. In accordance with equation 3.2.2, the equivalent input noise of the differential input stage can be written as:

$$V_{inp} = \frac{\sqrt{2}}{g_{m,N} \cdot r_{trn}} \cdot \sqrt{(V_{N,N} \cdot g_{m,N} \cdot r_{trn})^2 + (V_{N,P} \cdot g_{m,P} \cdot r_{trn})^2} \qquad (3.2.6)$$

where:

V_{inp} is the equivalent input noise voltage.

r_{trn} is the resistance of the output transistors.

$$r_{trn} = \frac{1}{g_{DS,MN2} + g_{DS,MP2}}$$

Rearranging eqn. (3.2.6) gives:

$$V_{inp} = v_{inp} \cdot \sqrt{2 \cdot \left(1 + e_r^2 \cdot \mu_r \cdot \frac{W_P \cdot L_N}{W_N \cdot L_P}\right)} \qquad (3.2.7)$$

where:

e_r is the relative noise factor

$$e_r = \frac{V_{N,P}}{V_{N,N}}$$

μ_r *is the mobility ratio of the free charge carriers*

$$\mu_r = \frac{\mu_P}{\mu_N}$$

Noise optimization of the differential input stage can be achieved by differentiation of equation 3.2.7. The relative minimum can be found by setting the first derivate to 0.

$$\frac{dV_{inp}}{dV_{N,N}} = 0$$

This results in:

$$L_N = L_P \cdot \frac{W_N}{W_P \cdot e_r^2 \cdot \mu_r} \tag{3.2.8}$$

The last equation combined with eqn (3.2.7) gives:

$$e_r^2 \cdot \mu_r \cdot \frac{W_P \cdot L_N}{W_N \cdot L_P} = 1 \tag{3.2.9}$$

Therefore, the N-channel and P-channel load transistors should be designed to achieve a symmetric behaviour of the equivalent noise voltage. Assume that measurements of the noise coefficient result in a value of X1 for 1/f noise and a value of X2 for the thermal noise component. Therefore the procedure presented above to minimize the 1/f noise figure or the thermal noise figure results in an optimization of the transistor length. Thus the evaluated length of the transistor can be written as:

$$L_{N,opt} \approx \frac{W_N}{W_P} \cdot L_P \cdot X1 \quad \textit{due to the 1/f noise component} \tag{3.2.10}$$

$$L_{N,opt} \approx \frac{W_N}{W_P} \cdot L_P \cdot X2 \quad \textit{due the thermal noise component} \tag{3.2.11}$$

Noise optimized comparators with sufficient DC gain result in very high accuracy. In A to D converters time continous comparators can be used that operate by charging or discharging of a capacitor, i.e. with a ramp. Time continous operation for high resolution requires an offset compensation technique that is independent of the signal line. In section 3.3 a design of an indirect chopper amplifier will be presented

that fulfils the demand of time continuity and very high DC-gain. Hence a combination of the low noise design procedure and indirect chopper concepts gives a time continous amplifier that can be used as a comparator for resolutions up to 16 bit.

3.2.3 Time Discrete Comparators

Time discrete comparators operate in different time windows. Mostly two time windows are in common use, i.e. the auto zero phase, which cancels the component offset, and the active phase, or the comparison phase. These time windows need to be implemented in the overall clocking scheme of the system. The next section presents a novel auto zero comparator concept that fulfils the demand, which is also stabilized against component offset, clock feed through offset errors and influences of the ringing of the power lines.

3.2.3.1 The Auto Zero Comparator

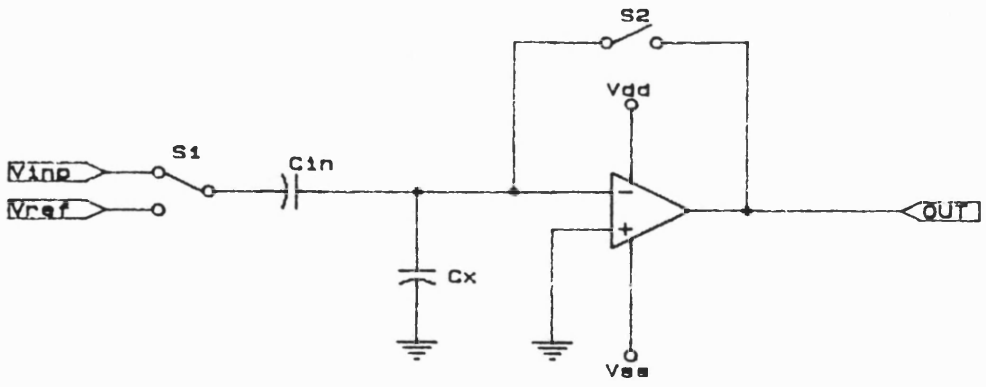

Figure 3.2.5 Auto zero comparator

Figure 3.2.5 shows the typical configuration of an auto zero comparator. The important design criteria will be discussed in detail. The two clock phases are the most important time schedules used in all clocked circuits presented later on.

Clock phase 1: Initialization

During initialization, the auto zero switch S2 is closed and the signal switch S1 is closed to Vref. Following compensation of the charges due to the reference voltage and the auto zero voltage, the voltage drop across the input capacitor can be written as:

$$V_{Cin} = V_{ref} - (V_{DD/2} + V_{Off}) \tag{3.2.12}$$

where: V_{Off} is the offset voltage of the inverter stage

The suffix b represents "before", i.e. the stabilized level before the comparison phase starts. The time constant τ due to the stabilization of the voltage V_{C1b} is defined as:

$$\tau = \frac{C + C_L}{g_m} \tag{3.2.13}$$

where: C is the internal output nodal capacitance of the inverter

C_L is the external load capacitance

where:

$R_{Source} \cdot g_{m,C} \ll 1$

R_{Source} is either the resistance of the input line or of the reference line.

Clock phase 2: Comparison

During comparison, the auto zero switch is open and the signal switch is closed to V_{inp}. The charge of the stabilized level within the comparison phase is given by:

$$V_{Cin} = (V_{inp} - V_{ref}) + (V_{Vdd/2} + V_{Off}) \tag{3.2.14}$$

The term $V_{DD/2} + V_{Off}$ in the equations 3.2.12/14 fix the operational point close to the midpoint voltage, that is 50% supply voltage. Therefore the decision of the comparator is mainly influenced by the term $V_{inp} - V_{ref}$. The slew rate of the comparator inverter can be calculated using:

$$\frac{dV_{out}}{dt} = \frac{g_m}{C + C_L} \cdot (V_{inp} - V_{ref}) \tag{3.2.15}$$

The gain factor is given by:

$$A = \frac{g_m}{C + C_L} \cdot T_K \tag{3.2.16}$$

where:

T_K is the comparison time

The transistor geometry can be derived by using eqn. (2.23):

$$\frac{W}{L} = \frac{2 \cdot g_m \cdot V_{GS,eff}}{B0 \cdot V_{GS,eff}^2 \cdot (1 + \alpha)} \tag{3.2.17}$$

The expected gain of standard inverters is in the range of 20 to 30 dB. A comparator capable of achieving a proper digital level using the specified minimum

resolution must have a minimum gain factor. To achieve this minimum gain, a stacked design technique is used. Three stages of auto zero inverters, separated by capacitances, are in common use to fulfil high resolution demands. Section 3.2.4 gives more detailed information about this technique.

3.2.3.2 Noise of an Auto Zero Comparator

Enz showed in Nov. 1984 [13], that the noise of an auto zero comparator is mainly influenced by the comparison period time. His description is very important in explaining the noise figures in clocked systems. Firstly, a time window function must be defined:

$$rect\frac{t-t1}{T} = 1 \;:\; t1-\frac{T}{2} \leq t \leq t1+\frac{T}{2}$$

$$rect\frac{t-t1}{T} = 0 \quad otherwise \tag{3.2.18}$$

where: T is the time period

The time dependence of the output voltage can be written as:

$$V_{out} = A0 \cdot (V_n((n+k)\cdot T) - V_n(t)) \tag{3.2.19}$$

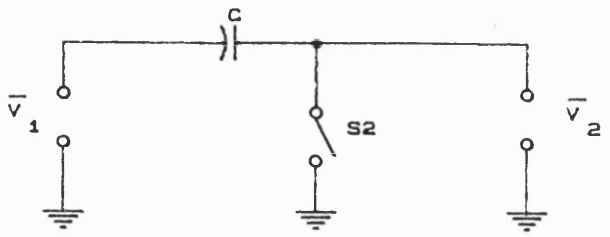

Figure 3.2.6 Equivalent circuit of an auto zero comparator

Figure 3.2.6 shows a transformed equivalent circuit of the auto zero comparator shown in figure 3.2.5, that simplifies the switched auto zero comparator behaviour. The switch S2 has the sample period frequency $f_s = 1/T$. Hence the output voltage can be defined as:

$$V2(t) = V1(t) - \sum_{-\infty}^{\infty} V1(nT) \quad rect\frac{t-(n+0.5)\cdot T}{T} \tag{3.2.20}$$

where: f is the actual signal frequency

The transfer function of the one stage auto zero comparator can now be written as:

$$H_n(f)^2 = (1 - si(\pi \cdot f \cdot T))^2 + \left(\frac{1 - co(\pi \cdot f \cdot T)}{\pi \cdot f \cdot T}\right)^2 \qquad : \quad n = 0$$

$$H_n(f)^2 = si^2 \cdot (\pi \cdot f \cdot T): \qquad n \neq 0 \tag{3.2.21}$$

where: si = sinx / x

co = cosx / x

The broadband input spectrum that is folded into the base band (low frequency - region) is therefore combined with the output spectrum because of the transfer function 3.2.21. Assuming that the input noise voltage is Gaussian distributed over the frequency range, then the average value of the output power spectrum is given as:

$$S1(f) = \sum_{-\infty}^{\infty} |H_n(f)|^2 \cdot S2(f - n \cdot f_s) \tag{3.2.22}$$

Equating 3.2.21 and 3.2.22 gives:

$$S1(f) = |H_0(f)|^2 \cdot S2(f) + si^2(\pi \cdot f \cdot T) \cdot S_{fold}(f) \tag{3.2.23}$$

where:

$$S_{fold}(f) = \sum_{-\infty}^{\infty \neq 0} S2(f - n \cdot f_s) \tag{3.2.24}$$

Eqn. (3.2.24) is valid, if the signal frequency f is above the baseband. With respect to the input noise, the amplifier can be simplified by a first order low pass function. Now the total input power spectrum equation can be rearranged to:

$$S2(f) = \left(1 + \frac{f_c}{|f|}\right) \cdot \frac{S_{n0}}{1 + (f/f_u)^2} \tag{3.2.25}$$

where: S_{n0} is the power of the thermal noise

f_c is the corner frequency of the amplifier (3dB)

f_u is the unity gain frequency of the amplifier (0dB)

f is the signal frequency

The noise equivalent bandwidth is given by:

$f_{noise} = \frac{\pi}{2} \cdot f_c$

Separation of the thermal noise and the 1/f noise gives:

$$S1_{kT/C}(f) \approx S_{n0} \cdot (|H_0(f)|^2 + \pi \cdot fu \cdot T \cdot si^2(\pi \cdot f \cdot T)) \quad (3.2.26)$$

where:

$S_{n0}|H_0(f)|^2$ *is the noise power of the base band*

$S_{n0} \cdot \pi \cdot fu \cdot T \cdot si^2(\pi \cdot f \cdot T)$ *is the noise power of the folding terms*

Within the Nyquist range, eqn. (3.2.24) can be rewritten as:

$$S_{fold}(f) = \int_0^{f_s/2} S2 \cdot (f - n \cdot f_s) df \quad (3.2.27)$$

If fu >> f_s then:

$$S_{fold}(f) \approx S_{n0} \cdot \frac{f_C}{f_s} \cdot \left(\frac{2 \cdot f_s^2}{f_s^2 - f^2} + \ln \frac{f_u^2}{(1.5 \cdot f_s)^2 - f^2} \right) \quad (3.2.28)$$

Inserting equation 3.2.28 into 3.2.23 gives the low frequency component of the output power noise spectrum within the Nyquist range:

$$S1_{1/f} \approx S_{n0} \cdot \left(|H_0(f)|^2 \cdot \frac{f_C}{f_s} + si^2(\pi \cdot f \cdot T) \cdot \frac{f_C}{f_s} \cdot 2 \cdot \left(1 + \ln \frac{f_u}{f_s} \right) \right) \quad (3.2.29)$$

The summation of equations 3.2.26 and 3.2.29 defines the broadband power noise spectrum:

$$S1(f) \approx S1_{kT/C}(f) + S1_{1/f}(f) \quad (3.2.30)$$

Due to the frequency terms in equations 3.2.26 and 3.2.29, it is obvious that the low frequency noise power is decreased in clocked circuits.

3.2.4 The Multi Stage Auto Zero Comparator

The multistage auto zero comparator is based on the concept presented before. The gain is increased due to the number of stages n and can be calculated from [14]:

$$A_n = \frac{1}{n!} \cdot \left(\frac{g_m \cdot T_n}{C} \right)^n \tag{3.2.31}$$

To minimize the influence of clock feed through errors, a sequential control of the auto zero switches is required. This sequential switch control starts with the closing of the first switch and ends with the closing of the last. Thus each clock feed through error is cancelled in the following stage. This procedure results in an effective offset just from the last stage. The relative error voltage after completion of the sequential switching is:

$$V_{err} = \frac{\Delta V_{Off} \cdot (n-1)!}{g_m \cdot T_n / C^{n-1}} \tag{3.2.32}$$

3.2.5 Cross Coupled Auto Zero Comparator

3.2.5.1 The Switched Cross Coupled Concept

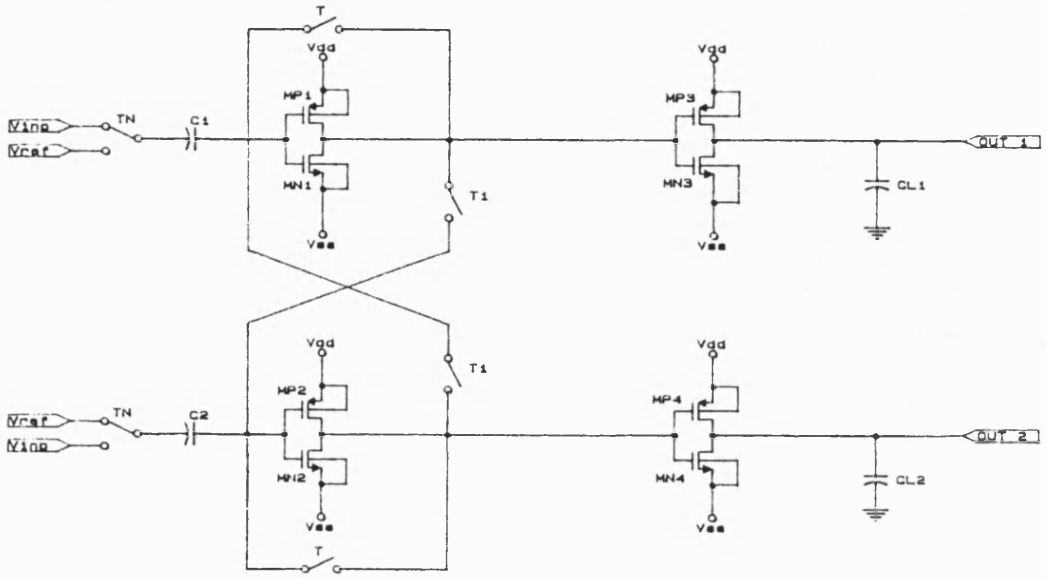

Figure 3.2.7 Switched cross coupled comparator

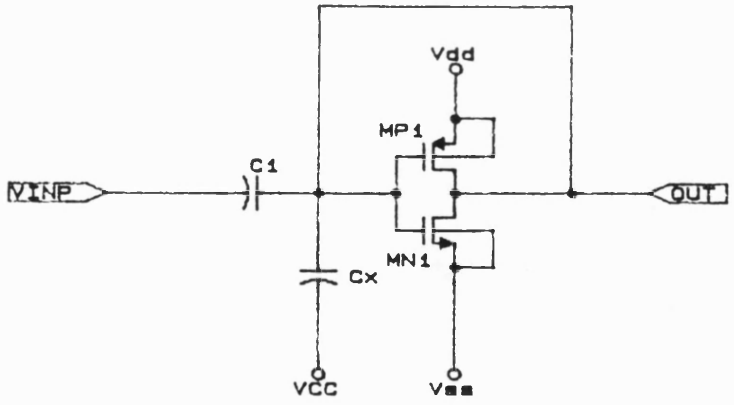

Figure 3.2.8 Auto zero comparator: Offset compensation phase

Cross coupling of comparators result in an improved gain factor. The cross coupling can be done as described in [15,16] with switches between two symmetric

auto zero inverters. Figure 3.2.7 shows the circuit drawing. Analysis of this comparator begins with the offset compensation period. From figure 3.2.8 the initial voltages can be written as:

$$\begin{aligned} V_{C1} &= V_{inp} - V_{Off} \\ V_{Cx} &= V_{ref} - V_{Off} \\ V_{Off} &= V_{dd/2} + V_{Off,inv} \end{aligned} \tag{3.2.33}$$

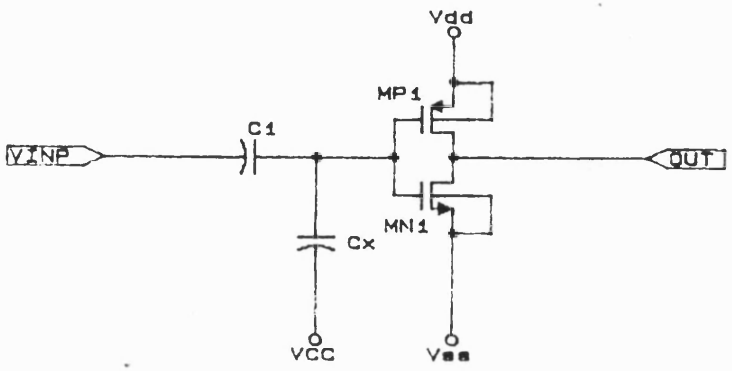

Figure 3.2.9 Auto zero comparator: Comparison phase

The comparison period is now described, using the equivalent circuit shown in figure 3.2.9. In order to avoid clock feed through effects of the cross coupled switches, this comparator requires a delay in closing the cross coupling switches during the comparison phase. This delay must be large enough for the output nodes to show a voltage larger than the clock feed through error voltage when the cross coupling switches close. This intermediate phase is called the actualisation phase. The full operation of the switched cross coupled comparator is as follows:

Phase1 : Auto zeroing (Offset cancellation)

Phase2 : Comparison and Actualisation (Decision of the digital level)

Phase3 : High gain mode (Fixing the digital level)

Phase 1 Auto Zero:

The overall input capacitance $C_{x1,2}$ is composed of the input capacitance of the inverter input C_{x1} and the capacitance of the interconnect line. Hence the input conditions across all elements can be evaluated as:

$$\begin{aligned} V_{inp,Amp} &= V_{ref} - V_{inp} + V_{Cx2} \\ V_{ref,Amp} &= V_{inp} - V_{ref} + V_{Cx1} \\ V_{C1} &= V_{inp} - V_{ref} + V_{Off} \\ V_{C2} &= V_{ref} - V_{inp} + V_{Off} \end{aligned} \tag{3.2.34}$$

Phase 2a: Actualisation

In this phase, the auto zero switches and the cross switches are open. The voltage at the output changes in respect to the gain factor of the amplifier. This can be described by:

$$\begin{aligned} dV_{out1} &= -\frac{g_m}{C_L} \cdot (V_{inp} - V_{ref})dt \\ dV_{out2} &= -\frac{g_m}{C_L} \cdot (V_{ref} - V_{inp})dt \end{aligned} \tag{3.2.35}$$

Phase 2b: High gain mode

The output nodes still have a voltage value that cannot be influenced by the

clock feed through error of the switches, hence the cross coupling switches can be closed. The overall output voltage change of this cross coupled inverter is calculated by using the propagation delay of both stages.

$$dV_{out1} = -\int_{t1}^{t3}\left(\frac{g_m}{C_L}\cdot V_{inp}\cdot\left(-V_{ref}-\int_{t1}^{t2}\frac{g_m}{C_L}\cdot(V_{ref}-V_{inp})dt\right)\right)dt$$

$$dV_{out2} = -\int_{t1}^{t3}\left(\frac{g_m}{C_L}\cdot V_{ref}\cdot\left(-V_{inp}-\int_{t1}^{t2}\frac{g_m}{C_L}\cdot(V_{inp}-V_{ref})dt\right)\right)dt \qquad (3.2.36)$$

where:

t1 is the start time

t2 is the propagation delay of the first inverter stage

t3 is the propagation delay of the second inverter stage

The solution of the equation system 3.2.36 gives:

$$V_{out,1}(t) = (V_{inp}-V_{ref})\cdot\left(e^{g_m\cdot\Delta t/C_L}-1\right)$$

$$V_{out,2}(t) = (V_{ref}-V_{inp})\cdot\left(e^{g_m\cdot\Delta t/C_L}-1\right) \qquad (3.2.37)$$

The auto zero comparator shows no charge conservation, because the input is clocked and no feed back to control a charge conservation process is included. Hence the circuit input capacitance C_x limits the accuracy of the input signal V_{inp}, because of the charge sharing effect. The input accuracy can be computed, and hence, the series capacitance at the input of the auto zero stage may be obtained directly. The voltage error of this charge splitting effect can be evaluated as:

$$q = \frac{C_{inp} \cdot C_x}{C_{inp} + C_x} \cdot (V_{inp} - V_{Off}) \tag{3.2.38}$$

The voltage drop across the gate input of the comparator can be derived by using the last equation.

$$V_{Cx} = \frac{q}{C_x} = \frac{C_{inp}}{C_{inp} + C_x} \cdot (V_{inp} - V_{Off}) \tag{3.2.39}$$

Rearrangement of eqn (3.2.39) and solving the new equation to achieve a expression $C_{inp} = C_x * X$ gives:

$$\frac{V_{inp}}{V_{Cx}} = \frac{V_{inp}}{V_{inp} - V_{Off}} \cdot \frac{C_{inp} + C_x}{C_{inp}} \tag{3.2.40}$$

$$C_{inp} = C_x \cdot \frac{V_{Cx}}{V_{inp} - V_{C_x} - V_{Off}} \tag{3.2.41}$$

$$C_{inp} = C_x \cdot X \tag{3.2.42}$$

The resolution of the comparator will be limited by noise and also by the maximum input node capacitance.

3.2.5.2 The AC - Cross Coupled Concept

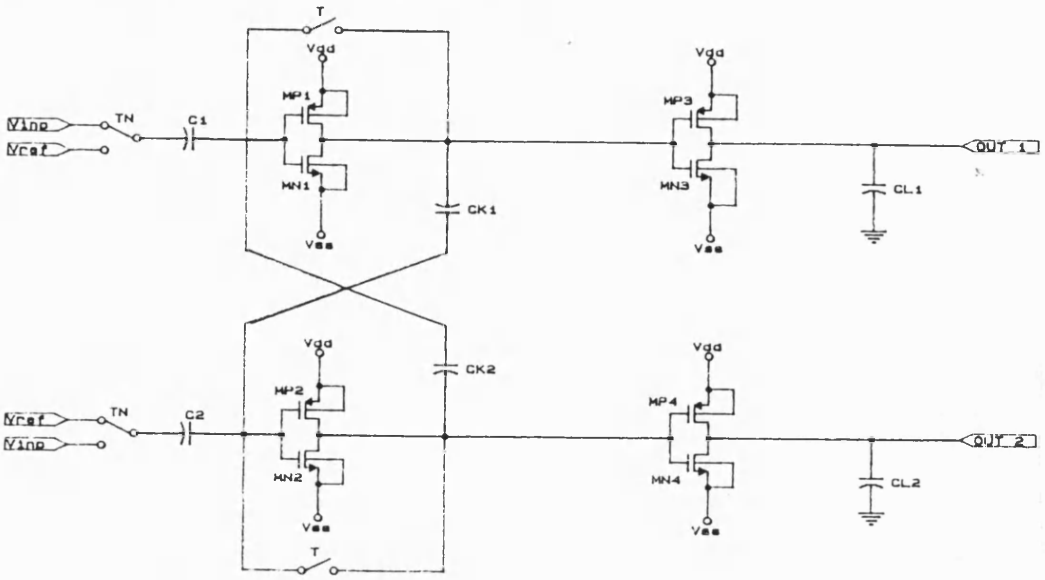

Figure 3.2.10 AC-cross coupled comparator

The study of the switched cross coupled concept shows a feedforward characteristic during phase 2. It is obvious that capacitances can be used to feed forward this cross coupled comparator. The advantage of using cross capacitances is that the clock feed through error voltage induced by the cross coupled switches may be neglected. Hence the use of cross capacitances leads to higher speed (direct feed forward effect) and a fully symmetrical comparator design, where any errors induced by the switches are perfectly minimized, because they occur on each side with the same characteristic [17,18]. Figure 3.2.10 shows the circuit drawing.

The calculations for this comparator are similar to the switched cross coupled design. The gain of the total system is based on the equation 3.2.31.

$$A = \frac{1}{2} \cdot \left(\frac{g_m \cdot T_C}{C} \right)^2 \qquad (3.2.44)$$

The transient characteristic of the output for one stage is given by:

$$dV_{out,a} = -(V_{inp} - V_{ref})\frac{g_m}{C}dt \tag{3.2.45}$$

Integration of equation 3.2.45 over the propagation delay time of both inverter stages results in the following expression for the ac cross coupled comparator:

$$V_{out} = \int_0^{t1}\left(V_{ref} - V_{inp} + \int_{\tau}^{t1+\tau} (dV_{out,a})\right)\frac{g_m}{C}dt \tag{3.2.46}$$

The comparison stage begins with a gain that is the product of the gain of the two inverter stages. The time dependent output voltage contributes to equation 3.2.46. Resolutions up to 16 bit may be obtained from this comparator concept.

Allstot and Black pointed out [19], that the sensitivity of capacitances due to ringing of the supply line (substrate) can be improved by 10dB, if the capacitors are laid out in their own well.

Dimensioning of the cross coupling capacitors is with respect to the charge times and to the damping characteristic (low pass characteristic) during the first few millivolt slews of the output node. Any ringing of the output during the first few mV change of the output at the beginning of the comparison phase can result in an unexpected decision of the comparator. Therefore, the cross coupled capacitances should be large enough to achieve a low pass characteristic with a time constant of about 30% of the low/high or high/low transient time. Based on experience, the cross coupled capacitances are about ten times the value of the input capacitances.

$$\Delta V_{inp,\min} = \pm\sqrt{R_n \cdot g_m \cdot \frac{kT}{C}} \tag{3.2.43}$$

where:

R_n is the input noise resistance

$$R_n = \frac{V_{Rn}}{4 \cdot k \cdot T \cdot \Delta f}$$

$$\Delta f = \frac{\pi}{2} \cdot f_{3dB}$$

Δf *is the input noise bandwidth*

3.3 Operational Amplifiers

Operational amplifiers (OpAmps) are one of the most important analogue building blocks in CMOS circuits. Table 1 shows the important parameters of opamps which directly effect the quality of CMOS circuits, along with typical values for the parameters.

1. CMRR PSRR (CMRR:common mode rejection ratio
   PSRR:power supply rejection ratio)
2. Amplification (60dB - 90 dB)
3. Sensitivity to capacitive loads (phase margins) and internal nodel capacitances (poles)
4. Offset (+/- 20 mV)
5. Settling time (10 *nsec to a few* µsec)
6. Slew rate (1 to 20 V/µsec)
7. Unsymmetric output control
8. Substrate biasing of n / p - channel transistors (limitation of common mode range)

Table 1 Important OpAmp parameters

The criteria shown above will be discussed in greater depth. In the literature, many special design features have been presented and discussed for improved circuit design. In view of the research into A to D conversion based on improved circuits, an operational amplifier must operate with and without an external load capacitor without influencing the stability criteria. Following Hosticka's publication of his dynamic OTA (Operational Transconductance Amplifier) concept in October 1980 [20], OTA's have been designed for use in loadless operation by using a dynamic biasing source. Dynamic biasing of the amplifier results in the normal operation condition when the dynamic bias source mirrors the maximum current into the amplifier input stage. In this mode, the input transistors operate in saturation. The resulting gain is overall in the range of 50 to 60 dB. The amplifier operates in high gain mode when the bias current decreases to the weak inversion current. This operating condition corresponds to the minimum output current. Hence the amplifier can operate loadless, in regard to the stability criterion, because the internal transconductance g_m is close to zero.

3.3.1 Common Mode Rejection and Power Supply Rejection Ratio

Most designs of opamps need both the load transistors and the bias source connected in series with the input transistors. Normally the linear input voltage range is about a threshold away from the supply rails, thus limiting the input voltage range. Another important factor is that the input transistors must operate within the saturation region. A design method will now be presented which achieves maximum input linearity. The drain currents of the two inputs are given by:

$$I_+ = g_{m1} V_{inp} \tag{3.3.1}$$

$$I_- = g_{m2} V_{inn} \tag{3.3.2}$$

where: $I_{+,-}$ are the branch currents of the input stage

$g_{m1,2}$ are the transconductances of the input transistors

V_{inp}, V_{inn} are the effective gate voltages of the input transistors

The input linearity range can be expanded by decreasing the bias potential. This forces the bias current source to become more inaccurate. The stability of the bias current source can be calculated as:

$$\Delta I = V_{Bias} \cdot \Delta g_m + g_m \cdot \Delta V_{off} = 0 \tag{3.3.3}$$

where:

$$\Delta V_{off} = \frac{\Delta g_m}{g_m} \cdot \frac{I_0}{g_m} \tag{3.3.4}$$

$$I_0 = g_m \cdot V_{Bias} \tag{3.3.5}$$

The term Δg_m signifies a nonideality of the input transistor transconductance. This nonideality can also be expressed, [21], as the difference between the drain to source currents of the input transistors:

$$\Delta I \approx g_m \cdot (V_{inp+} - V_{inp-}) \tag{3.3.6}$$

The input current common mode is given in respect to 3.3.6 as:

$$I_{CM} = \frac{(I+) + (I-)}{2} = \frac{V_{inp+} + V_{inp-}}{4R_{Bias}} \tag{3.3.7}$$

where: R_{Bias} is the resistance of the bias transistor

Equation 3.3.7 shows that the input differential stage ideally corresponds to differential signals. The finite bias current source forces the common mode behaviour of a differential input stage to be nonideal. This behaviour will be defined as the common mode rejection ratio CMRR. The definition of the CMRR is:

$$CMRR = \frac{differential \quad mode \quad gain}{common \quad mode \quad gain}$$

$$CMRR = \frac{\frac{\Delta I}{V_{inp-} - V_{inp-}}}{\frac{I_{CM}}{2 \cdot (V_{inp-} + V_{inp-})}} \tag{3.3.8}$$

The design goal of any differential input stage is to maximise the CMRR. The differential mode gain can be rewritten in terms of the small signal parameters as:

$$A_{dm} = \frac{g_{m,inp}}{g_{D,inp} + g_{Dload}} \tag{3.3.9}$$

or

$$A_{dm} = \frac{g_{DBias}}{2(g_{Din} + g_{Dload})} \tag{3.3.10}$$

where: A_{dm} is the differential mode gain

g_{Din} is the conductance of input transistor

g_{Dload} is the conductance of the load transistors

Equation 3.3.8 can now be rearranged :

$$CMRR = \frac{2g_{m,inp}}{g_{D,Bias}} = 2 \cdot \frac{(\frac{W}{L} \cdot V_{Geff})_{inp}}{(\frac{W}{L} \cdot V_{Geff}^2 \cdot l)_{Bias}} \qquad (3.3.11)$$

Equation 3.3.11 shows that an increase in the geometry ratio of the input transistors results in an increase in the CMRR. It must be noted that to achieve a small value of $g_{DBias,}$ a long bias transistor is required. Therefore the bias current must be held low and the input transistors must be designed with large geometries. In a later section 3.3.5.4 it will be shown that an increase in bias current results in larger bandwidth.

The power supply rejection ratio PSRR is defined as the ratio of the differential gain to the power supply gain, A_{PS}.

$$PSRR = \frac{differential \quad mode \quad gain}{power \quad supply \quad gain}$$

$$PSRR = \frac{A_{dm}}{A_{ps}} \qquad (3.3.12)$$

where: A_{dm} is the differential mode gain

A_{PS} is the power supply ringing gain

Power supply ringing contributes to the sensitivity of an amplifier via parasitic effects such as capacitances, interconnect lines and back biasing of transistors. PSRR will be analysed by taking into account the influence of V_{DD} and $V_{SS,}$ respectively. Ringing of the supply or ground line is like ringing of the bias tail current:

$$\frac{dV_c}{dV_{DD}} = \frac{-1}{2(g_{m,inp} + g_{m,Bias})} \cdot \frac{dI_0}{dV_{DD}} \qquad (3.3.13)$$

$$\frac{dV_c}{dV_{SS}} = \frac{1}{2(g_{m,inp} + g_{m,Bias})} \cdot \frac{dI_0}{dV_{SS}} \tag{3.3.14}$$

where: V_c is the output node of the input stage

The bulk terminals of the input transistors are connected to the common source node of these transistors. This is shown in figure 3.3.1. All the influences of the various gains that contribute to CMRR and PSRR are also frequency dependent. The overall gain of the amplifier is given by:

$$A_0 = A_{dm} \cdot \left(1 \pm \frac{1}{CMRR} + \frac{1}{PSRR}\right) \tag{3.3.15}$$

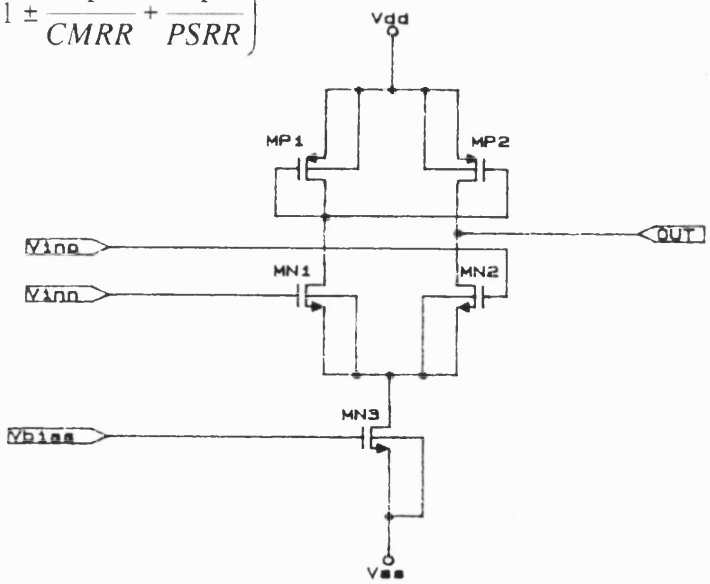

Figure 3.3.1 Input stage of an operational amplifier

Implicit in eqn (3.3.15) is that a signal voltage must be above the noise floor to achieve a proper response of the amplifier.

3.3.2 Slew Rate

Slew rate describes the time for a voltage transient to achieve a desired swing at the amplifier output. Normally the slew is defined for large signal behaviour. In the case of an OTA concept, the slew rate is defined as the current through the input current mirror transistors, multiplied by the current amplification factor required to load the overall output capacitance within a specified time. Hence the slew can be increased either by increasing the output transistor geometry or by increasing the bias tail current.

$$SR = 2 \cdot \left(\frac{I_{Bias} \cdot F}{C_{load}} \right) \tag{3.3.16}$$

The factor F is defined as twice the current amplification factor from input stage to output stage. The factor of two is included due to the two possible ways available to control the output stage symmetrically.

3.3.3 Offset

The offset is a continuous problem in the analogue field. Offset can only be minimized when the design is symmetrical. To achieve minimal offset condition in designing a differential input stage, the input transistors should be laid out in clusters. This means, that the input transistors are divided in few sections and the sections of the positive and negative input transistors are distributed over the silicon area. In this way any inaccuracy depending on the physical parameters will effectively be minimized due to the statistical variations over the total transistor area. Other offset errors occur due to strays of transistor parameters or parasitics, caused by the additional signal

mirror path required to control the n-channel output transistor in an OTA amplifier. To achieve high accuracy an offset calibration process is required. There are two ways to cancel the offset of an operational amplifier:

1. direct chopper stabilisation (auto zero technique)
2. indirect chopper stabilisation

3.3.3.1 Direct Chopper Stabilisation

The direct chopper stabilisation (auto zero offset technique) was presented in section 3.2.3. In some applications of operational amplifier designs, an additional input stage is required to cancel the offset. It is more convenient during the auto zero phase to bypass the output to the inverted input.

3.3.3.2 Indirect Chopper Stabilisation

In indirect chopping, as shown in figure 3.3.2, the signal path is time continuous and an additional auto zero nulling amplifier bypass is incorporated in the system.

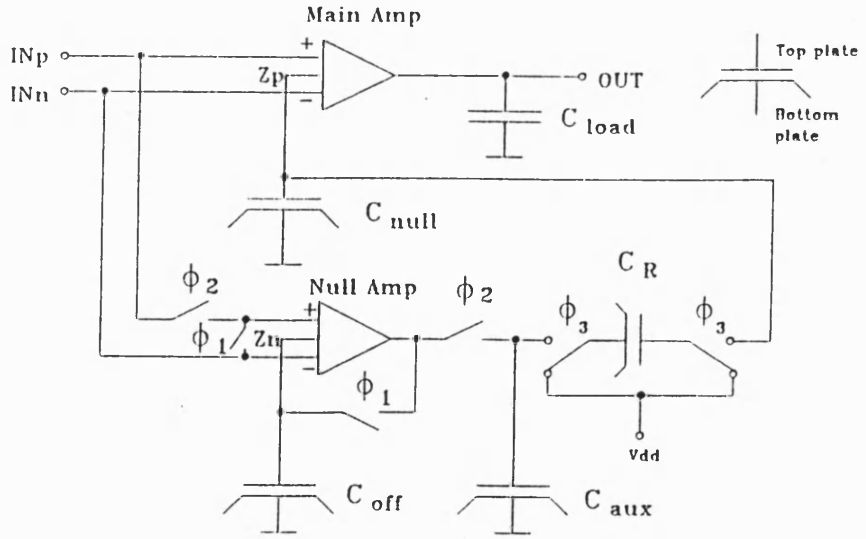

Figure 3.3.2 Chopper OTA

In general the chopper technique is a straight forward design based on the mechanical chopper implementation of Goldberg [21]. Coln [22] presented a useful chopper amplifier concept. Herein the offset voltage is shown to be reduced by the following relation :

$$V_{off,eff} = \frac{V_{off,N}}{A_N + 1} \tag{3.3.17}$$

where: A_N and $V_{off,N}$ are the gain and offset of the nulling amplifier.

Critical to this concept are the location of the pole of the auxiliary amplifier, the chopper frequency and the value of the auto-zero capacitance. The gain of the total system must have an OTA characteristic, i.e. the dominant pole of the system must be defined by the load capacitance. This means that the pole of the nulling amplifier must be carefully designed in order to match the ac-characteristic of the main amplifier. Matching in this sense can be done by controlling the chopper frequency. The chopper frequency must be close to the pole frequency of the main amplifier divided by the open loop gain of the auxiliary (nulling) amplifier. Therefore the nulling amplifier has a big time constant requiring a large capacitor. This is the disadvantage of the system, because this capacitor must be externally connected. The resulting gain in dB of the whole system is [22]:

$$A = A_N + A_M \quad (dB) \tag{3.3.18}$$

$$A = \frac{V_{out}}{V_{inp}} = \frac{V_{out}}{V_{inp} + V_{off,eff}} = A_N \cdot \frac{V_{out}}{V_{inp} + V_{off,M} + V_{off,inp}} \tag{3.3.19}$$

where A_M is the gain of the main amplifier.

Equation 3.3.19 shows that the offset is inversely proportional to the gain of the nulling amplifier. The RC network of the low pass section of the nulling amplifier can be usefully realised with a switched capacitor circuit. Maxwell showed in 1892 [23] that a periodically switched capacitor is equivalent to a normal ohmic resistor according to the relation:

$$R = \frac{T_{SC}}{2C} \tag{3.3.20}$$

The switched capacitor low pass filter in the indirect chopper operational amplifier concept of [22] shows that this technique seems to be applicable for circuits that require high accuracy and improved 1/f noise performances [24]. Assume that the nulling amplifier has a open loop gain of 40 dB and the main OTA has a unity gain bandwidth of 10 MHz with an open loop gain of 60dB, then the corner frequency of the dominant pole is at 10khz. The chopper corner frequency can be calculated as:

$$f_{ch} = \frac{f_{cf}}{A_N} \tag{3.3.21}$$

where

f_{ch} : chopper corner frequency

f_{cf} : corner frequency of the signal amplifier

For the example above:

$$f_{ch} = \frac{10kHz}{40dB} = 100Hz \tag{3.3.22}$$

choosing $C = 50pF$, *gives* $R = 2 \cdot 10^8 \Omega$

The time constant T must be designed with a safety margin, such that the resulting T never exceeds the corner frequency of the signal amplifier. The large resistor value could be designed with either a long transistor or a long transfer-gate. However, it is to be noted that this solution is worse in respect to the accuracy and reproduction aspects, due to the large variations of the transistor channel resistance. Thus it is not feasible to lay out such a resistor in a CMOS circuit with sufficient accuracy. It is obvious that the switched capacitor circuit is an alternative to this situation. The time constant of a SC - circuit is given by equation (3.3.20). In SC - circuits it is easy to compute the relation between the desired accuracy of the output voltage V_{out} and the switching time period t. The accuracy has an exponential behaviour based on the charge or discharge of the load capacitance:

$$V_{out} = -V_{inp} \cdot A0(1 - e^{-t/\tau}) \qquad (3.3.23)$$

where: A0 is the DC-gain

τ *is the time constant of the SC - circuit*

An accuracy of 1ppm is reached with a sample frequency of about 7 times bigger than the system's time constant.

The sample frequency $f_{s,ch}$ for the chopper amplifier is:

$f_{s,ch} \approx 7 \cdot f_{cf}$

So, for the example above:

$f_{s,ch} \approx 7 \cdot 100Hz = 700Hz$

Picking:

$f_{s,ch} = 1kHz$

gives, using eqn (3.3.20):

$$R = \frac{1msec}{2 \cdot 50pF} = 10^7\Omega$$

The time constant of the resulting lowpass is therefore:

$$T = R \cdot C = 10^7\Omega \cdot 50pF = 5 \cdot 10^{-4}\text{sec}$$

3.3.4 Stability Criterion

A well known and frequently used method of analysing the stability of analogue circuits is the Bode plot. This method is much easier to use than the Nyquist criterion in this work, because it can be invoked by the AC-analysis in BONSAI. Nyquist's theory for stability of a system is defined for open loop systems when the number of clockwise encirclements of the point (-1,0) is greater than the number of the poles defined by the transfer function of the system.

The stability criterion in the Bode method is easy to define using the Bode plot:

A system is stable if the phase margin at the transition frequency is large enough to take any parameter strays and load effects into account. The phase margin based on experience should be bigger than 20°. Phase margins less than this minimum value will force the system towards instability.

3.3.5 Development of a Chopper Stabilized Dynamic OTA

3.3.5.1 Design goals:

Unity gain bandwidth	: 10 Mhz
C_{Lmin}	: 20 pF
Phase margin (C_{Lmin})	: 30°
Slew rate (C_L=50pF)	: 5 V/μsec
Vdd - Vss	: 5 V
CMRR dc chopper	: 60 dB
PSRR +/- dc chopper	: 60 dB
A_{0min} (Chopper)	: 90 dB
$f_{chopper}$	: f_{cl}/A_V = 500 Hz
f_{SC-R}	: 4000 Hz
V_{off}	: <100μV

3.3.5.2 Designing the Bias Stage

Three standard bias sources exist for CMOS operational amplifiers. These are:

a. Two transistor	bias source figure 3.3.3
b. Widlar	bias source figure 3.3.4
c. Dynamic	bias source figure 3.3.5

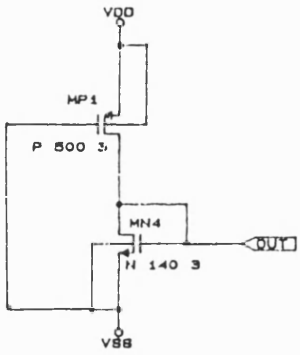

Figure 3.3.3

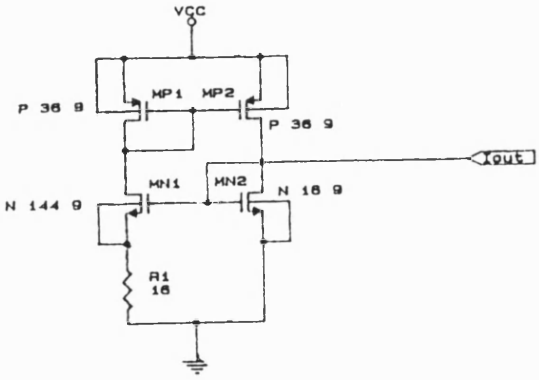

Figure 3.3.4.

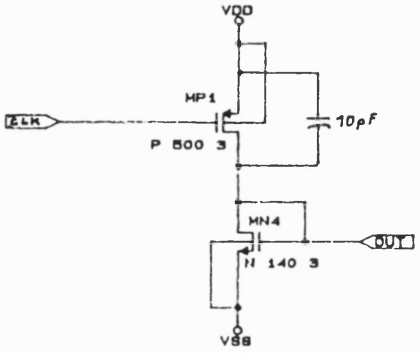

Figure 3.3.5

The two transistor bias source is never used for high accuracy circuits, as it is very sensitive to ripples in the supply lines.

3.3.5.2.1 Widlar Bias Source

The Widlar source [25] is almost supply independent. The design of this bias source has the criterion that the branch currents are identical. Therefore the effective gate-source voltage of the transistors MP1 and MP2 are identical. This forces the same geometry for both p- channel mirror transistors. The current in branch 2 will now be mirrored into branch 1. Deviations in the mirrored current are only influenced by strays in the transistors, i.e. threshold differences and geometry dependent strays. Close proximity of the transistors in the layout and unidirectional source and drain regions can minimize these influences. The control gate to source voltage of transistor MN2 is the voltage drop over the resistance R and the gate to source voltage of transistor MN1. The following equations outline the design of the bias stage of figure 3.3.4.

$$I_{ref} = \frac{B0}{2} \cdot \frac{W}{L_{MP2,1}} \cdot V_{Geff}^2 \tag{3.3.24}$$

$$\frac{W}{L_{MP2/1}} = 2 \cdot \frac{I_{ref}}{(B0 \cdot V_{Geff}^2)} \tag{3.3.25}$$

$$R \cdot I_{ref} = \sqrt{\frac{2 \cdot I_{ref}}{B0}} \cdot \left(\sqrt{\frac{1}{(W/L)_{MN1}}} - \sqrt{\frac{1}{(W/L)_{MN2}}} \right) \tag{3.3.26}$$

$$I_{ref} = \frac{2}{B0 \cdot R^2} \cdot \left(\sqrt{\frac{1}{(W/L)_{MN1}}} - \sqrt{\frac{1}{(W/L)_{MN2}}} \right)^2 \tag{3.3.27}$$

Transistor MN1 can be calculated using:

$$\frac{W}{L_{MN1}} = \frac{2 \cdot I_{ref}}{B0 \cdot (V_{Gseff,MN1} + V_R)^2} \tag{3.3.28}$$

The effective gate to source voltage can be easily derived from figure 3.3.4. The voltage drop across the resistor R gives the stability of the current source. Therefore the voltage drop across R should not be too small. Experience shows a good design value of V_R close to one threshold voltage, to avoid the entrance into the nonsaturation region of one of the transistors.

$V_R = V_{Tn}$

$$R = \frac{V_{Tn}}{I_{ref}} \tag{3.3.29}$$

$$\frac{W}{L_{MN2}} = \frac{2\ I_{ref} \cdot (W/L)_{MN1}}{\sqrt{2 \cdot I_{ref}} - \sqrt{B0 \cdot V_{Tn}^2 \cdot (W/L)_{MN1}}} \qquad (3.3.30)$$

The channel length calculation for a transistor operating in the strong inversion region can be done with the output conductance equation (see chapter 2). The following equation gives the drain current including the channel length modulation correction term.

$$I_{DS} = \frac{B0 \cdot W}{2 \cdot L} \cdot V_{Geff}^2 \cdot \left(1 + \frac{L}{L - L_D}\right) \qquad (3.3.31)$$

The calculation of the channel length with the equation 3.3.31 can be done using the first derivative of the drain current with respect to the drain to source voltage drop. In equation 3.3.31 the expression L_D is a function of V_{DS}. With equation 2.22 of chapter 2 equation 3.3.31 can be simplified to achieve an expression for g_{DS}.

Define:

$$A = \frac{B0 \cdot W}{2 \cdot L} \cdot V_{Geff}^2$$

$$B = \frac{K2 \cdot E_G}{2F}$$

$$C = -V_{DSS} + B^2$$

$$D = A \cdot L$$

$$E = L + K2 \cdot B/F$$

$$G = K2/F$$

where A to G are auxiliary variables, (F is a BONSAI correction factor for the channel length modulation constant K2)

$$I_{DS} = A + \frac{A \cdot L}{L - K2/F \cdot \sqrt{(V_{DS} + C)} - B} \tag{3.3.32}$$

$$\frac{\delta I_{DS}}{\delta V_{DS}} = \frac{dI_{DS}}{dV_{DS}} |_{V_{GS} = const,\ V_{BS} = 0,\ const} = g_{DS}$$

$$g_{DS} = \frac{d}{dV_{DS}} | A + \frac{D}{L + (K2 \cdot B)/F - K2/F \cdot \sqrt{V_{DS} + C}} | \tag{3.3.33}$$

$$g_{DS} = \frac{-D \cdot G/2 \cdot \sqrt{V_{DS} + C}}{E^2 + G^2 \cdot (V_{DS} + C) - 2 \cdot E \cdot G \cdot \sqrt{V_{DS} + C}} \tag{3.3.34}$$

From g_{DS}, an expression for the corresponding transistor length is developed.

$$X = 2\left(\frac{K^2}{F^2}\right) \cdot E_G - 2\left(\frac{K2}{F}\right) \cdot \sqrt{V_{DS} + C}$$

$$Y = \frac{K2^2}{F^2} \cdot \left(\frac{K2^2 \cdot E_g^2}{4 \cdot F^2} + V_{DS} + C + \frac{E_G \cdot K2}{F} \cdot \sqrt{V_{DS} + C} \right)$$

$$Z = \frac{B0 \cdot W \cdot V_{GS,eff}^2 \cdot K2}{2 \cdot g_{DS} \cdot F \cdot \sqrt{V_{DS} + C}}$$

where: X, Y, Z are auxiliary constants.

Finally, the minimal channel length is given as:

$$L = \frac{X \cdot \pm\sqrt{X^2 \pm 4 \cdot (Y - Z)}}{2} \tag{3.3.35}$$

Equation 3.3.35 can be simplified to:

$$L = \frac{\Delta V_{DS}}{\Delta I_{DS}} \cdot \frac{K2 \cdot I_{DS}}{2\sqrt{V_{DS} - V_{GS,eff}}} \tag{3.3.36}$$

To avoid channel length modulation effects within the circuit, the channel length should not vary. Therefore the design length is based on the transistor with the largest current amount.

Temperature effects can largely be neglected if equation 3.3.27 is solved by taking into account the temperature effects of the conductance constant B0 and the resistor. The temperature coefficients of the resistors (laid out in poly silicon or p - well) and the conductance constant B0 are equal and opposite. Equation 3.3.27 can be rearranged to solve this problem:

$$B0(25^o) \cdot B0(T) \cdot R^2(T) = B0 \cdot \left(\frac{T0}{T}\right)^{3/2} \cdot (R(1 + \Theta T))^2 \tag{3.3.37}$$

with Θ = temperature coefficient of the resistance material.

Θ can be a sum of some components, i.e. the resistor can be designed using a combination of poly and p-well.

3.3.5.2.2 Small Signal Analysis of the Widlar Current Source

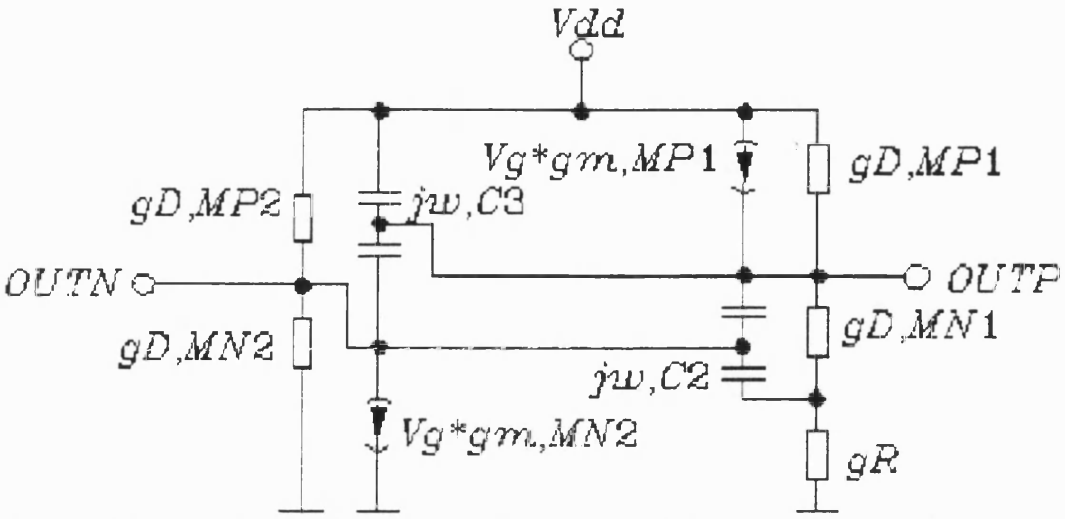

Figure 3.3.6 Small signal equivalent circuit of a Widlar current source

Figure 3.3.6 shows the small signal equivalent circuit of the Widlar current source. The relevant frequency dependent terms are influenced by the ringing of the supply voltage. The transistors MN1 and MP2 are most sensitive to power supply ringing. The complex conductances of both transistors MN1 and MP2 and the resulting drain current dependencies are given by the following equations:

$$g_{m,\ MN1/MP2} = j\omega C_{GS,\ MN1/MP2}$$

$$g_{DS} \approx \frac{\Delta I_{DS}}{\Delta V_{DS}}$$

$$g_{MN1/MP2} = g_{Ds,\ MN1/MP2} + j\omega C_{GS,\ MN1/MP2}$$

$$\Delta I_{DS} = \Delta V_{DS} \cdot \sqrt{g^2_{DS,\ MN1/MP2} + \omega^2 \cdot C^2_{GS\ MN1/MP2}} \cdot e^{j\ \Phi} \qquad (3.3.38)$$

where:

Φ is the phase angle.

$\omega = 2\pi f$

f is the actual signal frequency

3.3.5.2.3 Dimensioning the Widlar Constant Current Source

The current source to be used in the chopper amplifier is specified as follows:

$V_{dd} = 5V \pm 0.5V$

$I_0 = 50\mu A$

Using eqns (3.3.24 to 3.3.42) a minimum transistor length of 8 μm is calculated. The transistor length used will be 9 μm. This gives a low g_{DS} value and hence a stable current source. Table 3.1 shows the geometries of the elements according to figure 3.3.4.

MP1 = 36/9

MP2 = 36/9

MN1 = 144/9

MN2 = 16/9

R = $16K\Omega$

Table 3.1 Geometries of the Widlar current source.

3.3.5.3 Dynamic BIAS Source

The dynamic biasing [20] is based on charge or discharge of the bias capacitor. Figure 3.3.5 shows the design of a dynamic bias stage. This design is implemented in the amplifier design discussed here. In figure 3.3.5, the capacitor is connected in series with the bias transistors. In order to provide sensitivity of power supply ringing a stacked mirror technique is used. This design operates in the bias active phase as a normal bias source with a constant current mirrored into the amplifier bias transistor.

The passive phase is the loadless weak inversion mode. In dynamic biasing concepts the clock period depends on both the load time of the output capacitor and the capacitor value of the bias stage.

The dynamic current i can be defined as:

$$i(t) = i_0 e^{-t/\tau} \tag{3.3.39}$$

where:

$$\tau = \frac{2C}{B0 \cdot W/L \cdot (V_{Geff})} = \frac{2C}{B0 \cdot W/L \cdot (V_{GS} - V_{T0})} \tag{3.3.40}$$

The dynamic current period starts with the saturation current of the bias transistors, followed by weak inversion.

The amplification, A_{dyn} and the pole frequency, f_{pol} of the dynamic biasing can be written as a time dependent function:

$$A_{dyn} = A_0 \cdot (1 + t/\tau) \tag{3.3.41}$$

$$f_{pol} = f_{pol0} \cdot \left(\frac{\tau}{\tau + t} \right)^3 \tag{3.3.42}$$

where:

$f_{pol,0}$ is the pole frequency according to the on-resistance R_{on} of the bias transistor.

The design of the geometry of the components of a dynamic current source is mainly a matter of experience and experimental simulation. The design goal for a dynamic current source is for it to achieve, within a specified active time window, the same average current as its static equivalent.

3.3.5.4 Designing the OTA

In the literature, the design of circuits corresponding to particular geometries is often disregarded. This section shows a possible way to design an operational amplifier in respect to the design goals shown above. Some of the calculations will be done in accordance to [26].

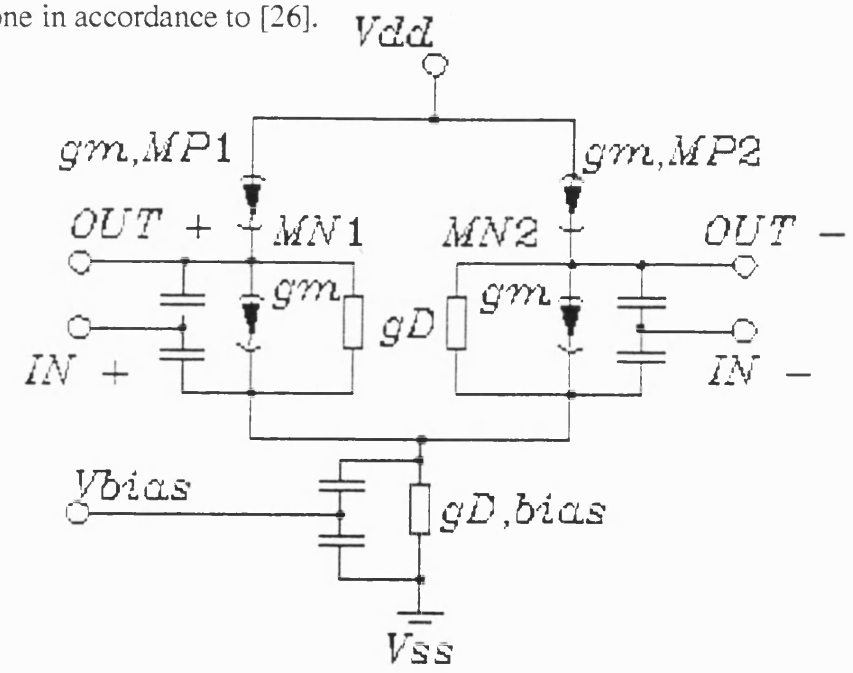

Figure 3.3.7 Small signal equivalent circuit of the OTA input stage

Figure 3.3.7 shows the small signal equivalent circuit input stage of an OTA amplifier. First, the bias source current is selected. The transistors operate in saturation. The input bias current I_B is split into an I_{Diff1} branch and an I_{Diff2} branch.

$$I_B = const = I_{Diff1} + I_{Diff2} \tag{3.3.43}$$

$$dI_B = 0 = dI_{Diff1} + dI_{Diff2} \tag{3.3.44}$$

The small signal equivalent circuit in figure 3.3.7 shows that the bias source is independent of the differential current. Therefore the bias source is neglected in the calculations. Each branch of the input stage is an active transistor loaded common source circuit. The input transistors are controlled by the voltages V + and V -, both referenced to V_{SS}. The load transistors can be defined by their ohmic resistances, R_{L1} and R_{L2}.

$$R_{Li} = \frac{V_{DS\ \ MP1}}{i_3} = \frac{1}{g_{m\ \ MP1} + g_{DS\ \ MP1}} \tag{3.3.45}$$

$$R_{L2} = \frac{V_{DS\ \ MP2}}{i_4} = \frac{1}{g_{m\ \ MP2} + g_{DS\ \ MP2}} \tag{3.3.46}$$

With respect to the small signal behaviour, the voltage drop of the input transistors can be derived as:

$$V_{DS1} = -\frac{g_{m\ \ MN1} \cdot R_{L1}}{1 + g_{DS1} \cdot R_{L1}} \cdot V - \tag{3.3.47}$$

$$V_{DB2} = +\frac{g_{m\ \ MN2} \cdot R_{L2}}{1 + g_{DS2} \cdot R_{L2}} \cdot V + \tag{3.3.48}$$

The combination of these two groups of equations results in:

$$V_{DS1} = -\frac{g_{m\ MN1}}{g_{m\ MP3} + g_{DS\ MP1} + g_{DS1}} \cdot V - \tag{3.3.49}$$

$$V_{DS2} = -\frac{g_{m\ MN2}}{g_{m\ MP2} + g_{DS\ MP2} + g_{DS2}} \cdot V + \tag{3.3.50}$$

$$i_1 = \frac{g_{m\ MP1} + g_{DS\ MP1}}{g_{m\ MP1} + g_{DS\ MP1} + g_{DS1}} \cdot g_{m,MN1} \cdot V - \tag{3.3.51}$$

$$i_2 = \frac{g_{m\ MP2} + g_{DS\ MP2}}{g_{m\ MP2} + g_{DS\ MP2} + g_{DS2}} \cdot g_{m,MN2} \cdot V + \tag{3.3.52}$$

Differential input stages are designed symmetrically. Therefore the changes of the current force a change of the voltage drop and vice versa:

$$\Delta i = g_m \cdot \Delta V$$

$$\Delta i = (g_{m\ MP1} + g_{DS\ MP1}) \cdot V_{DS\ MP1} \tag{3.3.53}$$

Using equation (3.3.11), the transistor geometries can be calculated as:

$$\frac{W/L_{inp}}{W/L_{Bias}} = \frac{2g_{m\ inp} \cdot V_{geff^2 Bias} \cdot (1+\alpha)}{g_{D\ Bias} \cdot V_{geff\ inp}} \tag{3.3.54}$$

The design criteria for the bias transistor are influenced both by the output current and also the current amplifification from the input to output stages. In the design example, the slew rate, SL, is given as 5 V/μ sec for a 50pF load capacitance. The output current can now be written as:

$$I_{out} = \frac{C_{L,eff} \cdot \Delta V_{out}}{\Delta t} = \frac{C_{L,eff} \cdot \Delta V_{out} \cdot SL}{\Delta V_{out}} = C_{L,eff} \cdot SL \qquad (3.3.55)$$

The design of the output stage is dependent on the slew rate and, of course, on the load capacitor $C_{L,eff}$. Because the slew rate is dependent on the load capacitor and the internal capacitances, a good design approach, based on experience, is to take $C_{L,eff}$ as:

$$C_{L,eff} = 2 \cdot C_L$$

where: $C_{L,eff}$ is the effective load capacitance which is the summation of the external load capacitance and the diffusion capacitances. For later use it is easier to abbreviate $C_{L,eff}$ as C_L.

The design of the output transistor geometries are derived from the charge transfer:

$$Q = C_L \cdot \Delta V = I_L \cdot \Delta t$$

$$I_L = \frac{B0}{2} \cdot \frac{W}{L} \cdot V_{GSeff}^2 \cdot (1 + \alpha)$$

$$\frac{W}{L} = \frac{2 \cdot I_L}{B0 \cdot V_{GSeff}^2} \cdot \frac{1}{(1+\alpha)}$$

where: Q is the charge to load the output capacitance

α is the channel length modulation

The current amplification between the input and output stages is given by the ratio of the transistor geometries, because the effective gate to source voltages are identical. Hence the current amplification is directly given by:

$$\left(\frac{W}{L}\right)_{inp} = K \cdot \left(\frac{W}{L}\right)_{out}$$

The bandwidth of the amplifier is as follows:

$$f_\tau = \frac{g_{m\ inp}}{C_L} = \frac{1}{C_L}\sqrt{\left(\frac{B0}{2} \cdot I_D \cdot \frac{W}{L}\right)_{inp}} \qquad (3.3.56)$$

The geometry and the current flow through the input stage are related by:

$$\frac{W}{L}_{inp} = \frac{2 \cdot f_\tau^2 \cdot C_L^2}{B0 \cdot I_{D\ inp}} \qquad (3.3.57)$$

$$I_{D\ inp} = \frac{I_{Bias}}{2}$$

Equation (3.3.54) must be compared to the result of the input transistor geometry calculation. The geometry of the bias transistor is given by:

$$\left(\frac{W}{L}\right)_{Bias} = \left(\frac{W}{L}\right)_{inp} \cdot g_{D\ Bias} \cdot V_{Geff,\ Bias}^2 \cdot (1+\alpha) \qquad (3.3.58)$$

Current mirror load transistors are designed with respect to the maximum current flowing through one branch of the input stage. The transistors have to operate in saturation. Therefore the geometries are calculated to give:

$$\left(\frac{W}{L}\right)_{L1/2} = \frac{2 \cdot I_{D,\ max}}{B0 \cdot V_{Geff}^2} \tag{3.3.59}$$

3.3.5.5 Discussion of CMRR

The next parameter to be dicussed is the common mode rejection ratio, CMRR. In equation (3.3.11), it was shown that common mode rejection is dependent on the geometry relationship between the input transistors and the bias transistor.

$$\left(\frac{W}{L}\right)_{inp} = \left(\frac{W}{L}\right)_{Bias} \cdot \frac{CMRR \cdot (V_{Geff}^2 \cdot I)_{Bias}}{2 \cdot V_{Geff,inp}} \tag{3.3.60}$$

The load transistor geometry depends on the maximum current in each branch. The branch current will be mirrored into the output stage via the load transistor of the input stage.

3.3.5.6 Discussion of the Output Stage

The standard output stage of an OTA is a two transistor amplifier controlled by current mirror transistors. The amplification factor A_{OTA} and the transition frequency f_τ are given by:

$$A_{OTA} = g_{m,MN2} \cdot \frac{g_{m,MP4}}{g_{m,MP2}} \cdot r_{out} \tag{3.3.61}$$

$$A_{OTA} = g_{m,MN2} \cdot \frac{W_{MP4}}{W_{MP2}} \cdot r_{out} \tag{3.3.62}$$

where: $L_{MP2} = L_{MP4}$

r_{out} is the output resistance

$$f_{\tau} = \frac{g_{m,inp}}{C_L} \tag{3.3.63}$$

Equation (3.3.62) shows that the amplification depends on the conductance of the output stage. Longer transistors result in a higher amplification factor. Channel length modulation effects contribute to the accuracy of equation (3.3.61), such that the current mirror factor $g_{m,MP4}$ / $g_{m,MP2}$ should not exceed a factor between 10 and 20. Improved output amplification can be obtained with the help of a cascode stage. The second term in equation (3.3.62) gives the output resistance. In [27] the weak inversion maximum amplification $|A0_{max}|$ is given by:

$$|A0_{max}| = \frac{\pi \cdot \varepsilon_{Ox} \cdot L}{\varepsilon_{Si} \cdot t_{Ox}} \tag{3.3.64}$$

The weak inversion amplification is higher than the strong inversion amplification, but the amplifier is unable to charge the load capacitor because of the extremely low weak inversion current.

In [20,28] a cascoded OTA is presented. The cascode transistors are controlled by a gate voltage fixed to signal ground. An advanced cascode design will be presented to fulfil the dynamic characteristic. This characteristics is of the forced weak inversion operation of the amplifier bias control and output section, achieved by a current mirror technique. The basic idea of the current control cascode (CCC) is that all of the current mirror transistors have the same effective gate voltage and therefore the same backbiasing within the dc-operation at midpoint voltage. Figure 3.3.8 shows the design of the new cascode stage. The calculation of the transistor geometries must be done using current mirror rules. The transistor length is the same as that used in the OTA input stage.

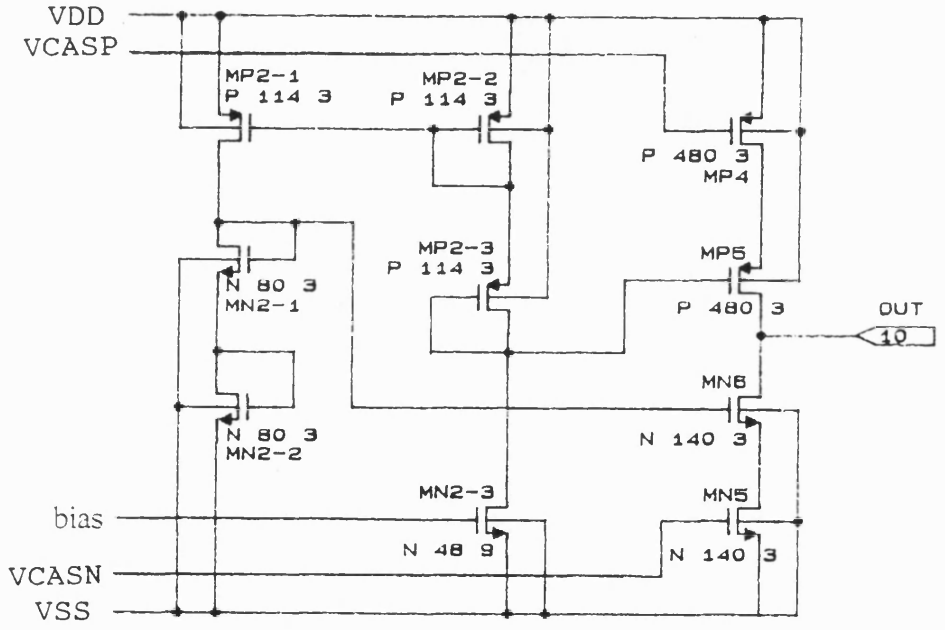

Figure 3.3.8 OTA cascode stage

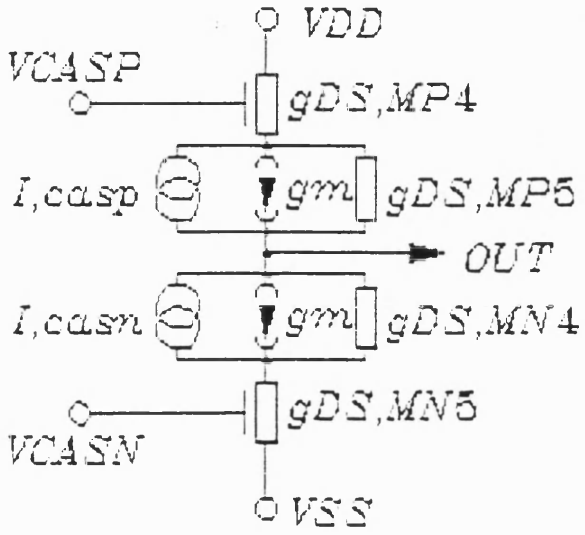

Figure 3.3.9 Equivalent circuit of the OTA cascode stage

Figure 3.3.9 shows the equivalent circuit of a cascoded output stage. To implement this equivalent circuit into the design of the CCC-OTA, R_L is converted to the equivalent expression of the conductance for both transistors MP5 and MN4. Therefore R_L can be written as:

$$R_L = \frac{1}{g_{DS\ MP4} + g_{DS\ MN5}} \tag{3.3.65}$$

Using eqn. (3.3.61) the transfer function can be calculated if the CCC is made symmetric.

$$H_{OTA} = g_{m\ MN2} \cdot \frac{g_{m\ MP4}}{g_{m\ MP2}} \cdot r_{out} \tag{3.3.66}$$

$$r_{out} = R_L \cdot 2 \cdot \frac{g_{m\ MP5}}{g_{DS\ MP5}} \tag{3.3.67}$$

where H_{OTA} is the transfer function of the OTA and r_{out} is the overall output resistance.

The transfer function (eqn. 3.3.66) can be written in the complex frequency domain, using the pole - zero arrangement:

$$H(p) = H_{OTA} \cdot \frac{(1 + p/z_1) \cdot (1 + p/z_2)}{(1 + p/p_i) \cdot (1 + p/p_2)} \tag{3.3.68}$$

The poles and zeroes of eqn. (3.3.68) are:

$$P_1 = -\frac{1}{C_L} \cdot \frac{2 \cdot g_{DS\ MP4} \cdot g_{DS\ MP5}}{g_{m\ MP5} + g_{DS\ MP5}} \tag{3.3.69}$$

$$P_2 = -\frac{g_{m\ MP2}}{N} \tag{3.3.70}$$

where:

$$N = \frac{C_{GD\ MP5} + C_{GD\ MP4}}{g_{m\ MP5} + g_{DS\ MP5}}$$

$$z_1 = \frac{g_{m\ MP4}}{C_{GD\ MP4}} \tag{3.3.71}$$

$$z_2 = -\frac{g_{m\ MP5} + g_{DS\ MP5}}{C_{MP4} + C_{bulk\ MP5}} \tag{3.3.72}$$

The equations above are accurate given the conditions:

$$g_{m\ MP4} = g_{m\ MN5}$$

$$g_{m\ MP5} = g_{m\ MN4}$$

$$g_{DS\ MP4} = g_{DS\ MN5}$$

$$g_{DS\ MP5} = g_{DS\ MN4}$$

These conditions provide a good design basis. The transistor geometries are dependent on the current mirror amplification factor. Equation 3.3.69 shows that a minimum load capacitance is required to get sufficient stability.

The slew rate of this amplifier can be calculated according to section 3.3.2:

$$SR = \frac{I_{DS\ MP1}}{C_L} \cdot \frac{W/L_{MP4}}{W/L_{MP2}}$$

The Bode plot of the amplifier gives the final analysis in respect to the stability criteria. The phase margin should be better than 20°.

3.3.6 A fully Differential Chopper Stabilized OTA

Following the design principles shown above and in [24], the remainding clock feed through error can further be minimized by using a fully differential operational amplifier including the chopper principle. This concept, shown in figure 3.3.10. needs two separated low pass filter bypass routes. Additionally the PSSR and CMRR characteristics are also improved by this design technique [29].

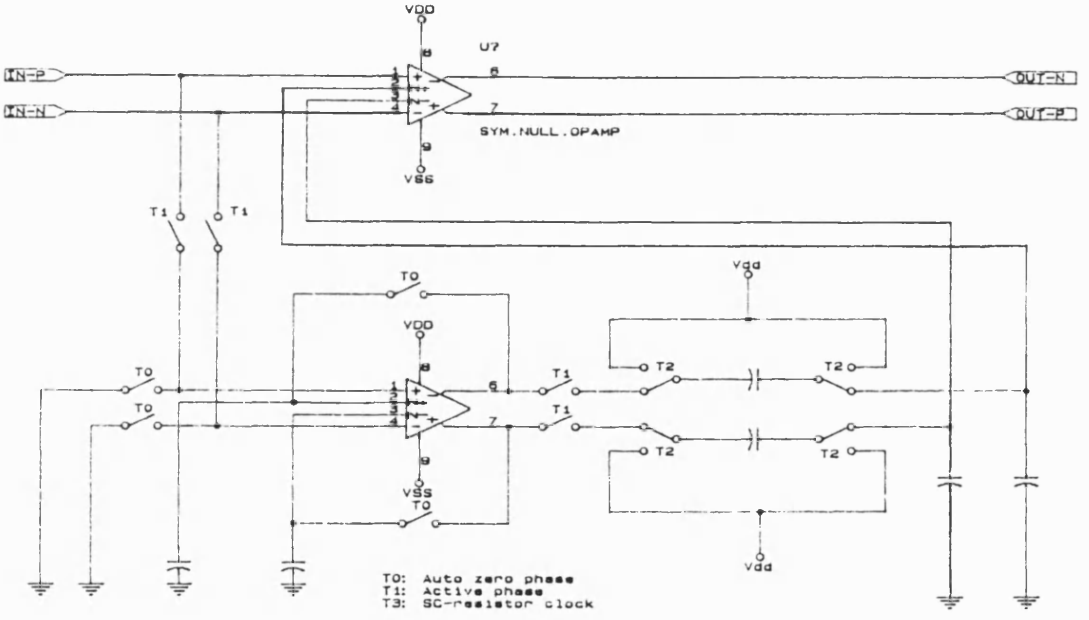

Figure 3.3.10 Fully differential chopper stabilized OTA

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CHAPTER 4

4. ANALOGUE TO DIGITAL CONVERTERS

4.1 Introduction

Acquisition of data for use in digital systems normally requires a data converter, because most of the data are analogue signals. A signal is analogue if the information in the signal is time continuous and amplitude dependent. A digital signal is time discrete and the signal information is usually split into three levels: High, Low and High - Impedance. A circuit that interfaces the analogue world with the digital world is an analogue to digital converter (ADC). The representation of the analogue information after completion of the A to D process is in the form of a digital word. The following section presents an overview of signal sampling, CMOS applicable A to D principles, characteristics of ADCs and the errors occurring in ADCs.

4.2 Signal Sampling

Transformation of a time continuous input signal into a train of digits means that the input signal must be chopped (sampled) at discrete time points. Figure 4.1 shows the principle of sampling an analogue signal.

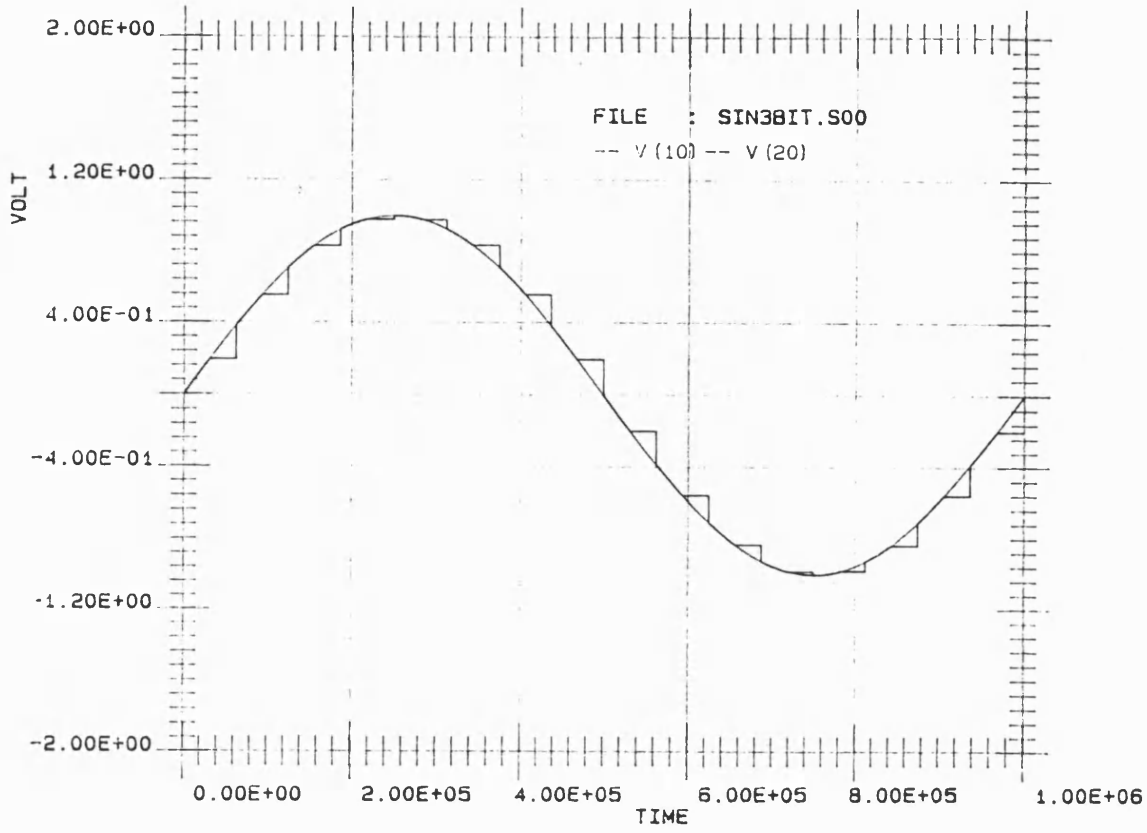


Figure 4.1 1 kHz sine wave sampled at 20 kHz

Any signal x(t) can be described in the frequency domain by its Fourier integral X(f).

$$X(f) = \int_{-\infty}^{\infty} x(t) \cdot e^{-j\omega t} dt \qquad (4.1)$$

The analogue information is transformed into the sampled information. x(t) represents the original signal.

The idealized sample train is a Dirac comb, that is a series of pulses with infinitely narrow pulse width following:

$$\int_{-\infty}^{\infty} \delta(t)dt = 1 \tag{4.2}$$

The pulses sampled with the Dirac comb can be described as:

$$v(t) = \sum_{-\infty}^{\infty} \delta(t - nT) \tag{4.3}$$

where:

T is the period time

The signal can now be represented by the following relation:

$$x_s(t) = x(t) \cdot v(t) = x(t) \sum_{-\infty}^{\infty} \delta(t - nT) \tag{4.4}$$

Fourier transformation of eqn. (4.4) gives:

$$X_s(f) = \sum_{-\infty}^{\infty} X(f - nF_T) \tag{4.5}$$

where: $F_T = \frac{1}{T}$

Real sample pulses have a pulse width of finite duration (rectangular shape) of time interval τ. In this case eqn. (4.5) should now be rewritten:

$$X_s(f) = \sum_{-\infty}^{\infty} \frac{\sin\frac{n\cdot\pi\cdot\tau}{T}}{\frac{n\cdot\pi\cdot\tau}{T}} \cdot F(f - nF_T) \tag{4.6}$$

Holding the signal after the sampling process gives with eqn. (4.6):

$$X_s(f) = \frac{\tau}{T} \cdot \frac{\sin(\pi\cdot\tau\cdot f)}{\pi\cdot\tau\cdot f} \cdot \sum_{-\infty}^{\infty}(f - nF_T) \tag{4.7}$$

Fig. 4.2 shows the Fourier spectrum of eqn. (4.7). This spectrum was produced using BONSAI (see chap.6) by sampling a 1 kHz sine wave at a sample rate of 20 kHz and was Fourier transformed using the "MURF" program [23].

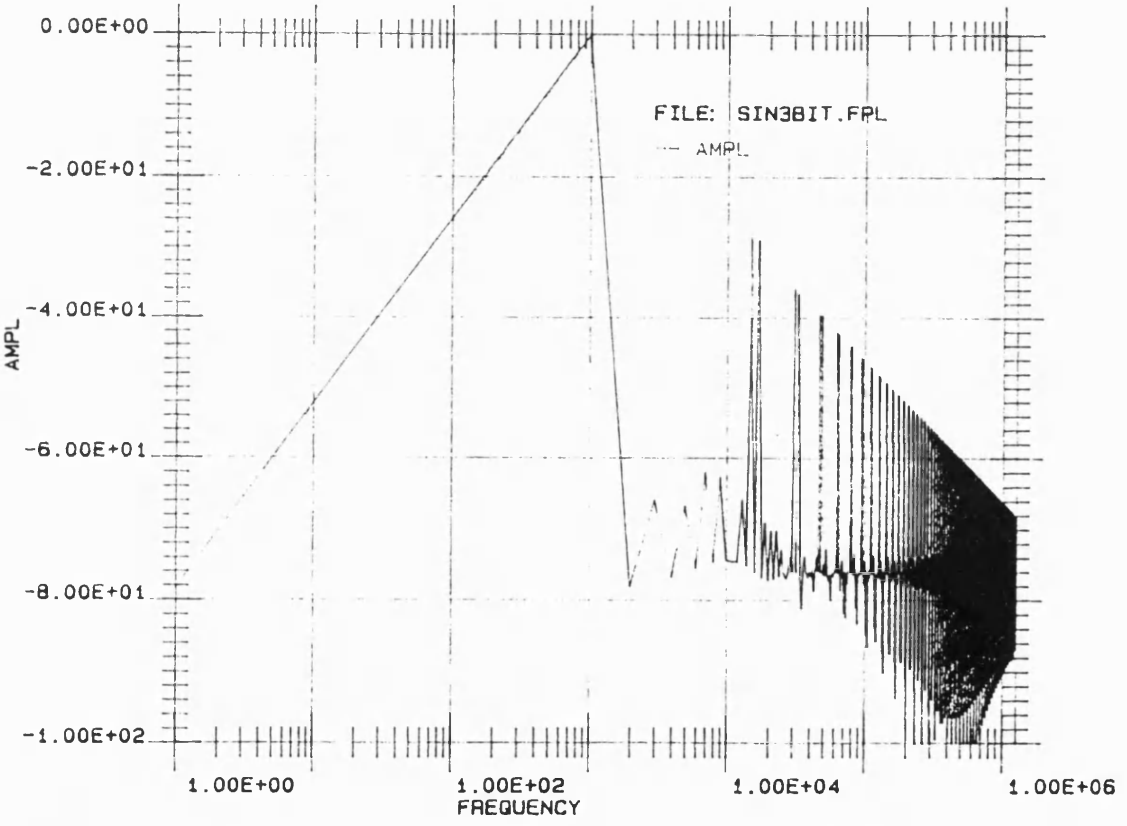


Figure 4.2 Fourier plot of a 1kHz sinewave sampled with 20kHz

Since the Fourier spectrum should only contain one line at 1 kHz, the resulting distortion can be seen. This distortion limits the accuracy and obviously the resolution in A to D systems.

4.3 Characteristics of ADC's

4.3.1 Transfer Function

The conversion of an analogue signal into a digital word results in 2^n digital levels for any n-bit A-D converter. The transfer function represents the analogue voltage as a function of the weighted bits:

$$V_{inp} = V_{ref} \cdot \left(\frac{B0}{2} + \frac{B1}{4} + \frac{B2}{8} + \ldots + \frac{BN}{2^{N+1}} \right) \tag{4.8}$$

where:

V_{ref} is the reference voltage

N = 0,1,2,...

Each digit (level) has a step width

$$V_{step} = \frac{V_{ref}}{2^n} \tag{4.9}$$

The change of the digital information occurs in the middle of each voltage step and can determined by:

$$V_{step} = V_{inp} + \frac{1}{2} \cdot \frac{V_{ref}}{2^n} \tag{4.10}$$

The connections of the digitized midpoints of each digital word represent a straight line with its origin at $V_{in} = V_{in/min}$ and digital word $D_0 = n$ (see fig. 4.4).

4.3.2 Resolution

The resolution is the smallest sampled input voltage step that can be detected. The resolution of an ADC gives the number of digits and the width of transition steps. Therefore the resolution can be written as

$$r = \frac{1}{2^n} \tag{4.11}$$

The comparator and the component matching have the most effect on the resolution (see section 4.6).

4.3.3 Accuracy

The accuracy is the difference between the ideal transfer characteristic and the real or measured transfer characteristic. In the section on errors in ADC some error sources contributing to the accuracy will be presented.

4.3.4 Conversion time

The conversion time is split into quantum conversion time and ADC conversion time. The ADC conversion time is often called the ADC cycle time. The quantum

conversion time is the time used from the sample time of the input voltage up to the update and acknowledge time-mark of the appropriate digital word. One A to D cycle is finished when the LSB accuracy is reached.

4.3.5 Nonlinearity

The nonlinearity is split into differential nonlinearity (DNL) and integral nonlinearity (INL). The DNL can be defined as:

$$DNL_i = \frac{V_{Bi} - V_{Bi-1}}{L_R} - 1 \tag{4.12}$$

where:

DNL_i: differential nonlinearity of the i-th level

V_{Bi} : voltage of the i-th level

V_{Bi-1}: voltage of the (i-1)st level

$$L_R = A \cdot l_r$$

where:

A = Amplitude of sinusoidal voltage

l_r = step width of voltage axis

From eqn. (4.12) the DNL represents the maximum difference in the size of a quantized step related to an ideal step.

The INL represents:

$$INL = \frac{measured \quad characteristic - ideal \quad characteristic}{L_R} \cdot LSB$$

Hence the INL gives the difference between the measured transfer characteristic and the ideal or best fitted straight line of the transfer curve.

4.3.6 Monotonicity

Monotonicity by definition requires an increase or decrease of the resulting digtal word over the full voltage input range. Non-monotonicity can only occur if the differential linearity error is equal or larger than 1 LSB. Figure (4.3) shows a typical monotonic failure. Mostly this failure occurs within the tolerance band of each conversion step.

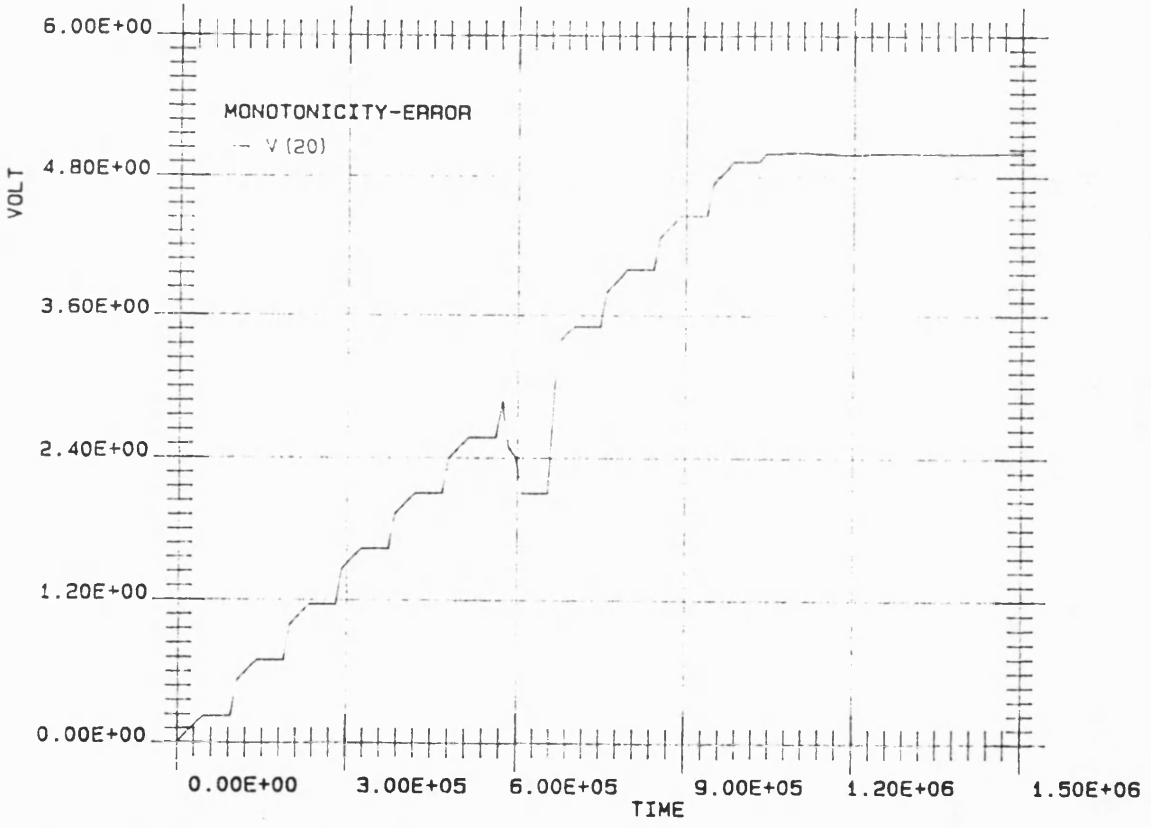


Figure (4.3) Monotonicity error

4.4 Errors in ADC's

4.4.1 Differential Linearity Error

This is the difference between two consecutive changes of the sampled input voltage and one quantum. If this difference is one quantum, the differential linearity error (DLE) is 0. For the maximum allowable DLE of half the quantum the variation of the output signal is within:

$$q - \frac{q}{2} \leq DLE \leq q + \frac{q}{2} \tag{4.13}$$

where:

q : 1 quantum

The DLE is often called the quantization error. Eqn. (4.13) shows the DLE centered to the mid-step transition of the analogue input voltage.

4.4.2 Offset Error

A parallel shift of the ADC transfer curve towards bigger voltage values can be considered as a system offset. Figure 4.4 shows the graph of the offset error related to the ideal transfer curve. This error can be minimized or cancelled by first measuring the system offset and then by calibration of the system.

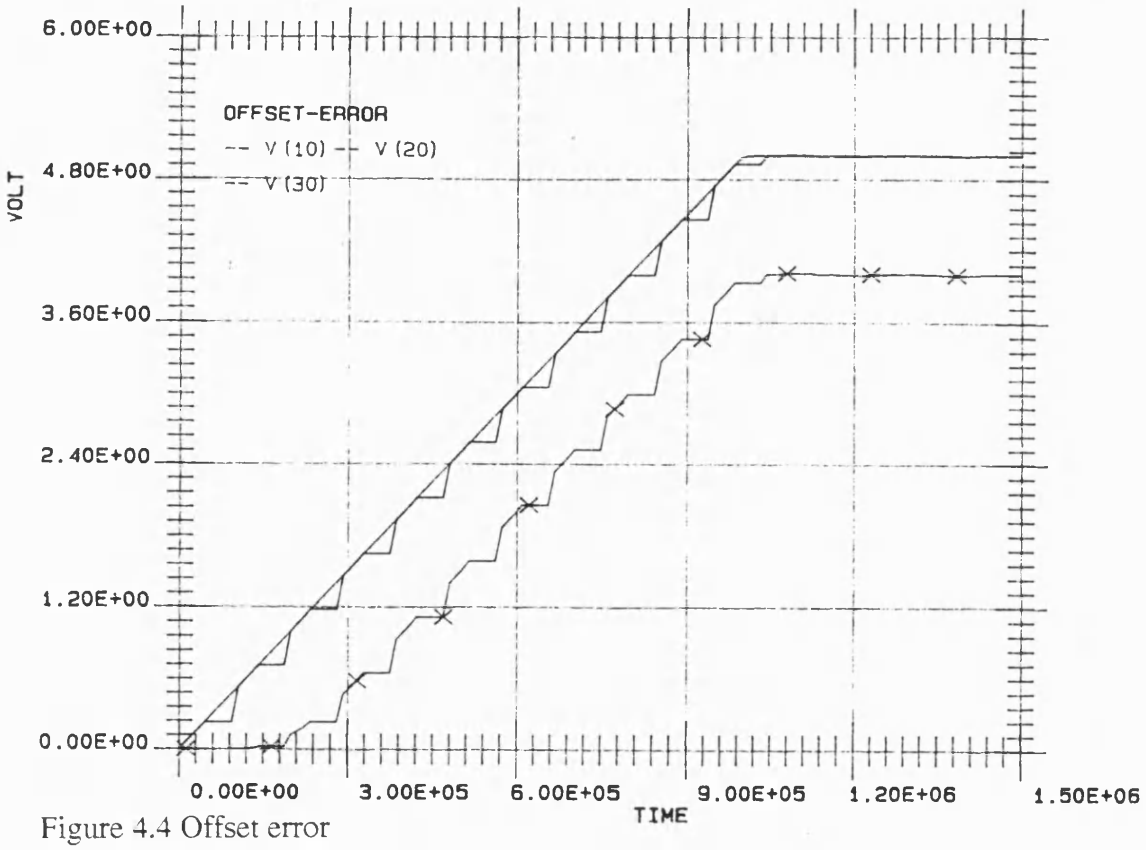


Figure 4.4 Offset error

4.4.3 Gain Error

This error, sometimes called a scale factor error, occurs if the converter operates monotonically but a coefficient failure is introduced. The following equation shows this error as a coefficient K in the transfer function.

$$V_{inp} = K \cdot V_{ref} \cdot \left(\frac{B0}{2} + \frac{B1}{4} + \frac{B2}{8} + \ldots + \frac{BN}{2^{N+1}} \right) \tag{4.14}$$

Values of K bigger than 1 result in a smaller step width, while values of K smaller 1 gives a bigger step width. Figure 4.5 shows the gain error influence related to the ideal transfer curve.

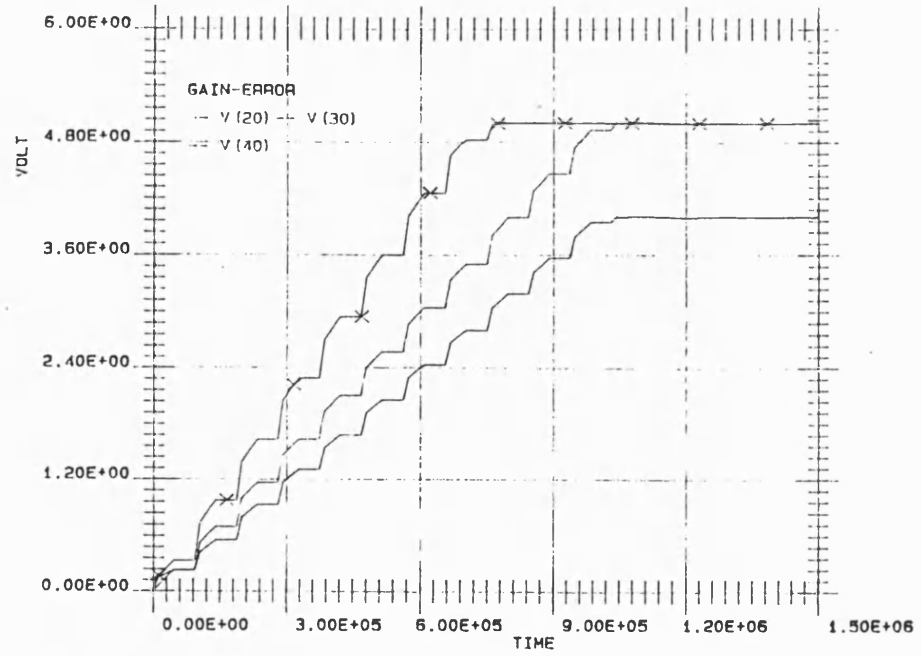


Figure 4.5 Gain error

4.4.4 Missing codes

This failure is an extreme linearity error and the result of a non-occurrance of an expected digital code. Missing code errors mostly occur in A to D array converters if the digit 0111... changes to 1000... that means half of the array capacitors will be redistributed. Figure 4.6 shows an error produced by missed codes.

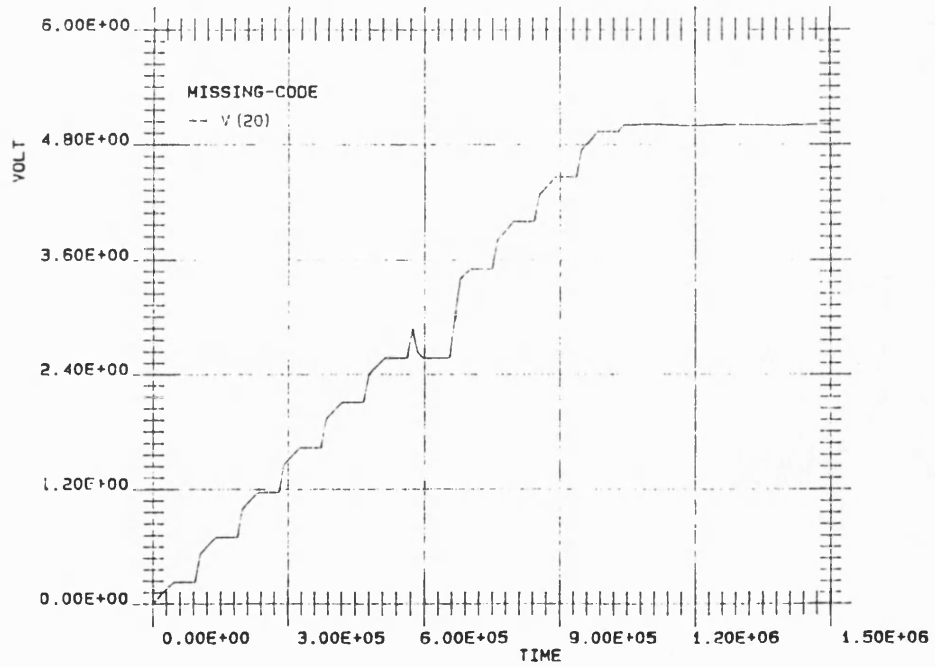


Figure 4.6 Missing codes

4.5 Measurement of ADCs

Two measurement procedures commonly used to characterize an A to D circuit are:

1.) The time domain procedure

2.) The frequency domain procedure

4.5.1 The time domain procedure

This procedure uses a reference circuit to control the ADC under test (AD-UT). It is obvious that the accuracy of the controlling DAC must be much better than the AD-UT. It has been shown [21] that an increment of 2 bits of the AD-UT needs an increment of up to 4 bits for the DAC circuit. The DAC output range must span the full specified range of the AD-UT. The data train of the AD-UT is monitored and is compared using a computer. The digital data train of the DAC and the resulting digital word of the AD-DUT are compared during each AD-step. Any failure occurance shown above is monitored, and can be analysed after test completion. The failure tolerances can be described as:

$$DAC: \qquad \Delta\varepsilon_{DAC} = \Delta LSB_{DAC} \cdot Step_{DAC} \cdot \frac{1}{2} \tag{4.15}$$

$$ADC: \qquad \Delta\varepsilon_{ADC} = \Delta LSB_{ADC} \cdot \frac{1}{2} \tag{4.16}$$

The term "$Step_{DAC}$" gives the number of LSBs, in terms of maximum DAC accuracy, for each DAC step. Eqn. (4.15) and (4.16) are compared:

$$\Delta\varepsilon = \frac{\Delta\varepsilon_{ADC}}{\Delta\varepsilon_{DAC}} = \frac{\Delta LSB_{ADC}}{\Delta LSB_{DAC}} \cdot \frac{1}{Step_{DAC}} \tag{4.17}$$

The resulting ADC step width must fulfil the condition

$$NLI \leq \Delta\varepsilon \leq NUI \tag{4.18}$$

where:

NLI means: Nearest Lower Integer

NUI means: Nearest Upper Integer

4.5.2 The frequency domain procedure

The frequency domain measurements can be examined using an FFT analyis. Firstly the sine wave of the generator is examined, then the digital information is converted to voltage values and analysed using an FFT program. Any inaccuracies in the A to D converter result in an increase of the noise floor of the ADC-FFT analysis. Windowing of the FFT data can reduce leakage effects, if arbitrary ratios of clock and analogue frequencies are used [19]. The signal to quantisation ratio (SQR) and the signal to noise ratio (SNR) are obtained directly from the FFT plot. It will be shown that examination of the FFT data stream using a linear regression fit gives a reasonable go-no go test.

The signal to quantisation ratio (SQR) can be described by using the uncertainty of the input voltage Vin(t) within each digitized interval of time duration T. Each digital transition is centralised so that the input voltage deviation $\varepsilon(t)$ is zero, when the input voltage has the same value as the appropriate digitized voltage. Hence this voltage deviation is maximized in the middle of each digital step (T/2 - point). The so defined error voltage can now be written within the ranges -T/2 to T/2 as:

$$\varepsilon_l(t) = -\frac{q}{2} \cdot \left(1 + \frac{t}{T/2}\right) \qquad -T/2 \le t \le 0 \tag{4.19a}$$

$$\varepsilon_u(t) = \frac{q}{2} \cdot \left(1 - \frac{t}{T/2}\right) \qquad 0 \le t \le \frac{T}{2} \tag{4.19b}$$

where:

$\varepsilon_{u,l}(t)$ is the upper and lower error voltage related to T/2.

q is the input voltage range of one digitized step.

T is the time interval of one digit

T/2 is the point within T, in which the digital information is changed by one digit.

The quantisation error $\bar{\varepsilon}^2$ can now be defined as the sum of the both voltage intervals ε_u and ε_l normalized to one time interval T.

$$\bar{\varepsilon}^2 = \frac{1}{T} \cdot \left(\int_{-T/2}^{0} \varepsilon_u^2(t)dt \quad + \quad \int_{0}^{T/2} \varepsilon_l^2(t)dt \right) \tag{4.20}$$

Inserting the equations (4.19a,b) into eqn (4.20) gives:

$$\bar{\varepsilon}^2 = \frac{1}{T} \cdot \left(\int_{-T/2}^{0} \left(\frac{q}{2}\right)^2 \cdot \left(1 + \frac{t}{T/2}\right)^2 dt \quad + \quad \int_{0}^{T/2} \left(\frac{q}{2}\right)^2 \cdot \left(1 - \frac{t}{T/2}\right)^2 dt \right) \quad = \quad \frac{q^2}{12} \tag{4.21}$$

The signal to quantisation ratio (SQR) is defined as:

$$SQR = \frac{E^2}{\bar{\varepsilon}^2} = 12 \cdot \frac{E^2}{q^2} \tag{4.22}$$

Using E for the full voltage range digitized by $E = q \cdot 2^n$ and inserting this expression in eqn.(4.22) gives:

$$SQR = 12 \cdot (2^n)^2 = 12 \cdot 4^n \tag{4.23}$$

Expressing eqn. (4.23) in dB:

$$SQR = 6.02 \cdot n + 10.79 \quad (dB) \tag{4.24}$$

Eqn. (4.24) is very important when examining the FFT results. A 4-bit A/D converter must fulfil a minimum SQR = 10.79 + 6.02 * 4 = 34.8 dB, a 5 bit A/D converter needs SQR ≈ 41 dB and so forth.

K. Uchida [20] showed that the spectral density of a full scale sine wave with N-bits can be described as:

$$S_{rms} = \sqrt{\frac{1}{T} \cdot \int_0^T \left(\frac{2^N}{2} \cdot q \cdot \sin(\omega \cdot t) \right)^2 dt} = \frac{2^N}{4} \cdot \sqrt{2}q \tag{4.25}$$

where:

q is the value of the LSB

The SQR of a sine wave can now be described as the ratio between its spectral density and the effective quantisation error $\bar{\varepsilon}$.

$$SQR_{sine} = \frac{S_{rms}}{\bar{\varepsilon}} = \frac{2^n}{2} \cdot \sqrt{6} \tag{4.26}$$

Expressing eqn (4.26) in dB gives:

$$SQR_{sine} = 6.02 \cdot n + 1.76 \quad (dB) \tag{4.27}$$

The signal to quantisation noise can be defined by different expressions because this SQR is dependent on shape of the quantized input voltage.

The signal to noise ratio (SNR) is defined as the ratio of the signal energy at a specified frequency, the fundamental frequency, to the total energy in the passband.

$$SNR = 10 \cdot \log \frac{W_S}{\sum_{i=f_{lo}}^{i=f_{up}} W_i - W_S} \tag{4.28}$$

where:

W_s is the energy of the fundamental frequency

$\sum W_i$ is the total energy of the passband

f_{lo} is the lower frequency limit

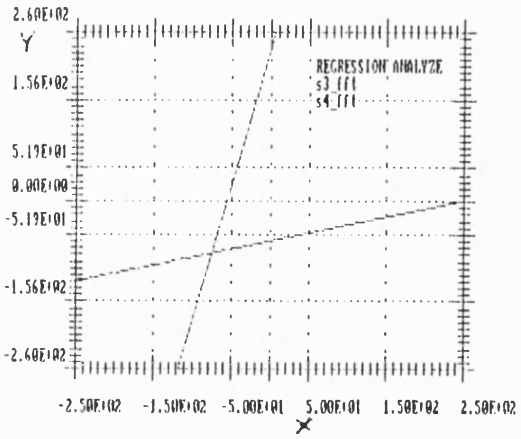
f_{up} is the upper frequency limit

Another parameter of interest in an A/D converter test result is the effective bit range, or effective resolution. Uchida defined the effective bit range of the ADC-UT as:

$$N_{eff} = N - \ln\left(\frac{E_{rms}(actual)}{E_{rms}(ideal)}\right) \tag{4.29}$$

The AD-test needs a pattern of such a form that all of the digits should be activated over one time period. A triangular shape of an input signal would fulfil this condition. Doernberg [21] showed that triangular shapes, because of their distortion characteristic, have a poor performance in FFT tests. He used a highly precise sine wave with ultralow distortion (<-95 dB). He points out that the sample frequencies must be nonharmonically related to the fixed sine wave frequency. This test procedure can be

performed if the fixed sine wave is sampled using a sample period much bigger than the conversion frequency of the test device. Hence only one sample frequency can be used. The spectrum of the test input must be monitored. The resulting output digital data train, converted to the appropriate voltage values, can now be Fourier transformed. This can be done either by a high speed DAC with an accuracy 2 to 4 times greater than the test device, or by data collection into a high speed RAM installed in the test set. After completion of the test, the RAM can be read out by a computer. After rearranging the digital data into their analogue voltage values, the FFT program can be used to transform the data into its spectrum. The spectrum of a golden device or an ideal computer simulated AD-converter shows the input frequency as the fundamental frequency, its harmonics and the convolved amplitudes of the fundamental frequency. The convolved amplitudes show a 20 dB roll off because of the nature of the sinx/x term. Any error occurances (nonlinearities, missed codes etc.) does not change the convolved parts, but the noise floor is raised. This phenomenom can be explained as an additional multiplication with a rectangular shaped voltage of a low amplitude (i.e. the error voltage). The FFT result gives no information about the failed bit. An easy method of a go-no go test is putting the data of a golden device and the data of the measured device together in a linear regression analysis. Perfect matching shows a regression coefficient of 1. Any error shows a decrease of the regression coefficient. The regression lines, the regression coefficient and the graphs of both regression lines are included in the TPLOT program [24]. Figure 4.7 shows the regression equations, the regression coefficient and the regression line plot.




```
REGRESSION ANALYZE   V. 1.3  W.TENTEN  GAMMERTINGEN 29.11.1988

FILE IDENTIFICATION

FILE 1: s3_fft  drawing line:  1
FILE 2: s4_fft  drawing line:  1

Linear-Regression : Y = -8.28E+01 +   2.47E-01 * x
                    avg dev x =  8.39E+00

Linear-Regression : X = -5.83E+01 +   2.38E-01 * y
                    avg dev y =  9.34E+00

Correlation coefficient     R = 0.24246
```

Figure 4.7 FFT-ADC-Test using the linear regression option of TPLOT

4.6 Noise in ADCs

Noise in ADCs is split into thermal noise, noise produced by the comparator and the overall noise figure of the converter. The noise figures of ADC's are examined by B.M.Gordon [22]. Gordon shows that the thermal noise error (see chap. 2) is produced by resistances (channels of MOS-FETs).

The comparator noise is defined by:

$$CNF = 20 \cdot \log \sqrt{\frac{\bar{e}_{ns}^2 + \bar{e}_{nc}^2}{\bar{e}_{ns}^2}} \quad (dB) \tag{4.30}$$

where:

CNF = Comparator Noise Figure

e_{ns} = noise voltage of source resistor or network resistance

e_{nc} = noise voltage generated by the comparator

Assuming the terms e_{ns} and e_{nc} are equal, then eqn. (4.28) simplifies to:

$$CNF = 20\log\sqrt{2} = 3 \quad dB$$

For examples the total RMS noise at the comparator input by a CNF of 3 dB is with a source impedance of 5KΩ and an active time window of 40 ns:

$$V_{rms} = \sqrt{2}\cdot 22.8\mu V_{rms} \quad = \quad 32.2\mu V_{rms}$$

The overall AD-converter noise figure ADNF is given by:

$$ADNF = CNF + PRNF$$

where:

ADNF is the AD Noise Figure

PRNF is Programming and Reference Noise Figure

The PRNF term represents the noise term generated by the elements of the complete ADC circuitry. Preferrably the noise of the impedance terms are generated by resistances and perhaps by the real part of capacitors. The influence of the complex part also seems to contribute to noise, due to leakage currents through the capacitor oxide. This influence is not well described in the literature.

Random noise effects are characterized by the uncertainties of the amplitude within a defined period of time. Generally this process is distributed with the Gaussian function, characterized by its mean value and the standard deviation. Generally the

distribution is centered at zero mean, with the amplitude scaled by a multiple of σ, the standard deviation. For example a 19.15% likelihood means a stray width within 0.5 σ range.

4.7 A to D Families

Different technologies, different applications and different tolerances result in innumerable A to D circuits. In [16] the most important families are described in detail. Some principles of A to D conversion applicable to CMOS technologies are now presented. The following section is a summary of these A to D principles.

4.8 CMOS A to D Principles

The design of Analogue to Digital Converters requires a number of analogue building blocks. All the circuits within the building blocks must be carefully designed when high accuracy is required. Care must be taken with parasitic effects of the components and with the influence of interconnections and terminals. (see Chap. 3)

CMOS design techniques have improved in this field since the middle of the 1970's. The literature used throughout this work was selected for CMOS applications and for the study of inaccuracies [1 to 22]. This list has been distilled down from a literature base containing many tens of references, too many to mention in this work. The most important A to D conversion techniques are :

1. McCreary principle of parallel charge redistribution [1,2]

2. Suaréz principle of serial charge redistribution [3,4]

3. Hamadé principle of voltage distribution with a serial resistor string and a switch

array. [3,15]

4. Fotohui principle which is a combination of the Mc.Creary and the Hamadé concept. [5]

5. Lee and Hodges principle which is an improved Fotohui design technique: MSB with resistor string, LSB with a capacitor array. [6]

6. Redfern principle, based on a combination of two serial connected resistor strings and two equivalent capacitors. [7]

7. Li, Shi and Gray principle of the cyclic algorithmic ADC. [8,9,10]

8. Delta Sigma principle. [11-14]

4.8.1 The Mc Creary Principle

Mc Creary published his A to D conversion concept based on charge redistribution in December 1975 [2]. Figure (4.8) shows the circuit drawing.

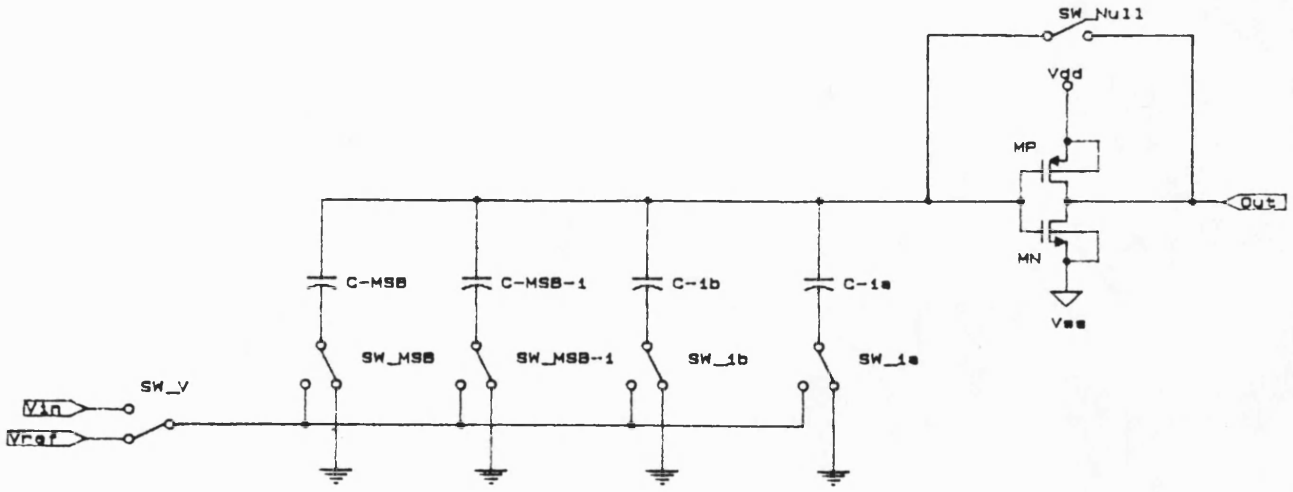


Figure (4.8) Mc Creary AD-Converter

This technique uses a binary weighted capacitor array and in addition one capacitor, weighted corresponding to the least significant bit. The binary weighted capacitor array has an increased accuracy compared to other concepts based on binary weighted resistor arrays. Relative strays of capacitor mismatches are much smaller than the resistor mismatches. This is the first step in increasing the accuracy of A to D converters. The Mc.Creary converter operates in three phases. The first phase is the sample mode:

Phase 1: Sample Mode

The capacitor array is connected with the bottom plates to the input voltage. The top plates, which are all connected to the input of the comparator, are grounded (at 50% supply voltage). The comparator can have its offset cancelled during this mode with a bypass switch from its output to its input. The charge, when the system is stable,is therefore given by the voltage 50% Vdd plus the comparator offset and the input voltage Vin. Related to the 50% Vdd point, the voltage over the total array is the difference between the input voltage and the offset voltage. Parasitic effects of the capacitors are only relevant on the input side. Normally the input voltage source charges the array as well as the parasitic capacitance, which is in parallel with the array. At the end of phase three it will be seen that the parasitic effect of the top plate is cancelled. Therefore this circuit technique is almost independent of parasitic effects.

Phase 2 : Pre - Redistribution

The pre/re-distribution phase is also called the hold mode. The connection from the top plate to 50% supply voltage is removed and the switches from the bottom plate to

the input voltage are all connected to 50% supply voltage. The input voltage connection is switched to the reference voltage. The stored charge is inverted during this cycle.

Phase 3 : Redistribution

The redistribution phase begins with the testing of the most significant bit (MSB). The switches of the capacitors are connected to V_{ref}, starting with the MSB switch, and continuing bit by bit with the other capacitors, ending with the least significant bit (LSB). During the redistribution phase, the capacitor array operates as a voltage divider. The digital decision, (bit n high or low) is made using the comparator decision.

The comparator output high: The input voltage V_{in} during A to D conversion is greater than the binary weighted reference voltage.

The comparator output low: The input voltage V_{in} during A to D conversion is smaller than the binary weighted reference voltage.

During each step the "bit" related switch is connected to V_{ref}, and the "bit-N" related switch remains in the V_{ref} connection, if the comparator detects that the input voltage exceeds the binary weighted reference voltage. The "bit-N" switch must connect to 50% V_{dd}, if the comparator detects an input voltage which is lower than the binary weighted reference voltage. The conversion proceeds in this way until all bits are checked. It is to be noted that all capacitors connected with their bottom plates to 50% V_{dd} during this phase are completely discharged. Therefore the original charge on the top plate is redistributed in the active capacitors after completion of the analogue to digital conversion cycle. The error charge of the top plate parasitic capacitor is nearly

zero, due to the redistribution of the original charge into the final capacitor configuration. That means that the error charge is weighted by the binary resolution. A 10 bit design has a remaining error voltage of approximately one thousandth of the top plate inaccuracy.

The accuracy is influenced by some other factors :

1. The variation of the oxide thickness contributes to inaccuracies of the capacitor values. Reduction of this error can be achieved if the capacitor array is designed with unity capacitor elements, the bigger capacitors framing the capacitors of lower values. The unity element is defined by the smallest capacitor (LSB) of the array. The two smallest capacitors are in the center of the array. This layout technique limits mismatches of the capacitors due to variations of the oxide thickness.

2. Etching of 90° angles can exacerbate underetching problems. The accuracy can be improved when the shapes used in the capacitor array have 45° angles.

3. Clock feed-through of the switches is not cancelled during the redistribution phase. Therefore care must be taken with the transfer-gate and the clock control circuits to keep the remaining clock feed-through charge as low as possible.

4.8.2 The Suárez Principles

In December 1975 R.Suárez published an A to D concept [4] based on charge sharing between two capacitors designed with the same size. The circuit drawing is shown in figure 4.9.

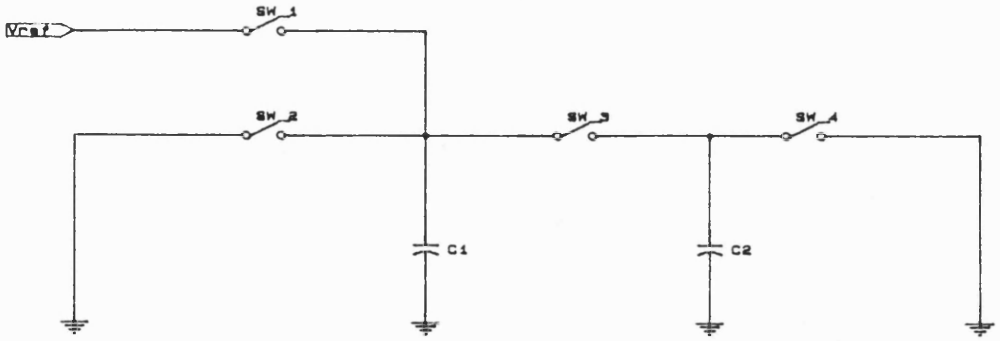


Figure 4.9 Suárez AD-Converter

The digital word will be detected within the following clock scheme:

The A to D conversion starts with the MSB.

Clock Phase 1.1

The input capacitor (C1) is loaded with the reference voltage equivalent to the positive power supply (V_{dd}). The other capacitor (C2) will be discharged during this cycle.

Clock Phase 1.2

Depending on the decision between the reference and the input voltage, the capacitor C2 remains discharged if the input voltage is below the reference voltage. Otherwise, the capacitor C2 will be charged with the reference voltage of the previous cycle. After this decision time, the charge redistribution between C1 and C2 ends the clock phase 2.1. (i.e. V_{dd} during phase 2.1). The clocks need to handle the intermediate charging of C2 as sub-phases within clock phase 2.

Clock Phase 2.1

The charge at the end of the previous clock phase remains as the new reference voltage.

Clock Phase 2.2

This clock phase is identical to clock phase 2.1.

This concept acts as a weighting A to D principle and is inherently monotonic. The accuracy is limited by the charging of parasitic capacitances as well as by errors induced by clock feed through. In a later chapter, an enhanced Suárez A to D converter will be presented.

4.8.3 The Hamadé Principle

In February 1976 Hamadé published his concept [15]. Figure 4.10 shows the circuit diagram.

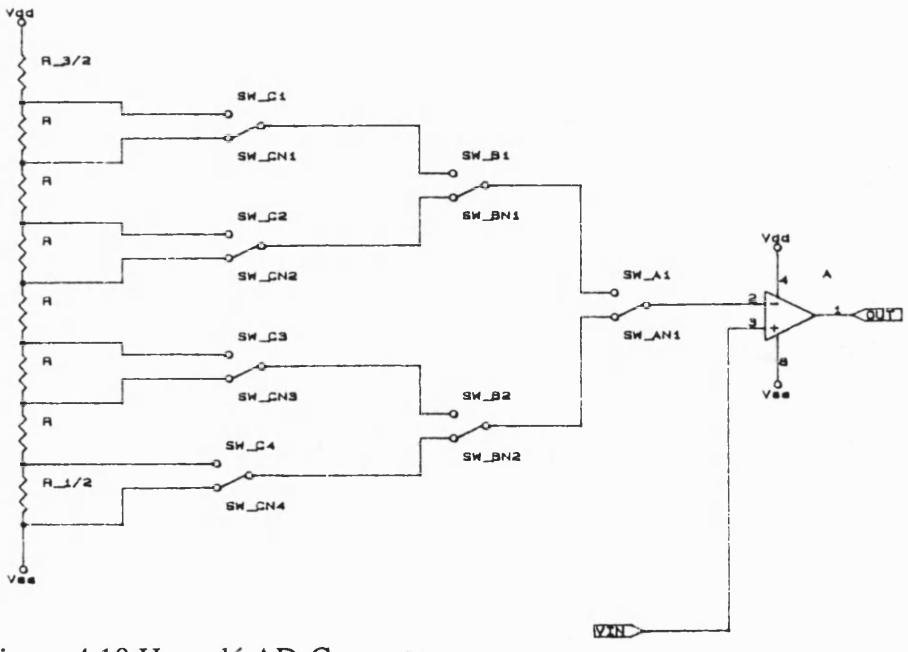


Figure 4.10 Hamadé AD-Converter

This principle is based on a resistor string in which the reference voltage is binary weighted. The comparison of the reference voltage with the input voltage will be done at the input of a comparator. The binary weight of the reference voltage within the resistor string is done with equal valued resistors. The tail end resistors are not equal to the internal resistor string. The upper resistor value is 1.5 times bigger than the internal resistor value and the lower resistor half the value of the internal ones. This is done due to the transition point of the digital output being centered on the midpoint voltage between neighbouring digits. The binary weight of the converter is realised with a switch array. The comparator decision is high if the input voltage exceeds the reference voltage. The relevant bit is set to "1". If the input voltage remains below the reference voltage, the relevant bit is set to "0". This principle is inherently monotonic.

Mismatches in the resistors generate inaccuracies of the binary steps and therefore lack of linearity in this approach. Clock feed-through of the switches is almost irrelevant, because this concept has no charge transfer elements. The offset error of the comparator limits the resolution. High resolution with this design requires a long resistor string and a lot of switches. Due to this, the design is only of interest for A to D converters with a small number of digits/bits.

4.8.4 The Fotohui Principle

B.U.Fotohui introduced his concept in December 1979 [5]. Figure 4.11 shows the circuit drawing.

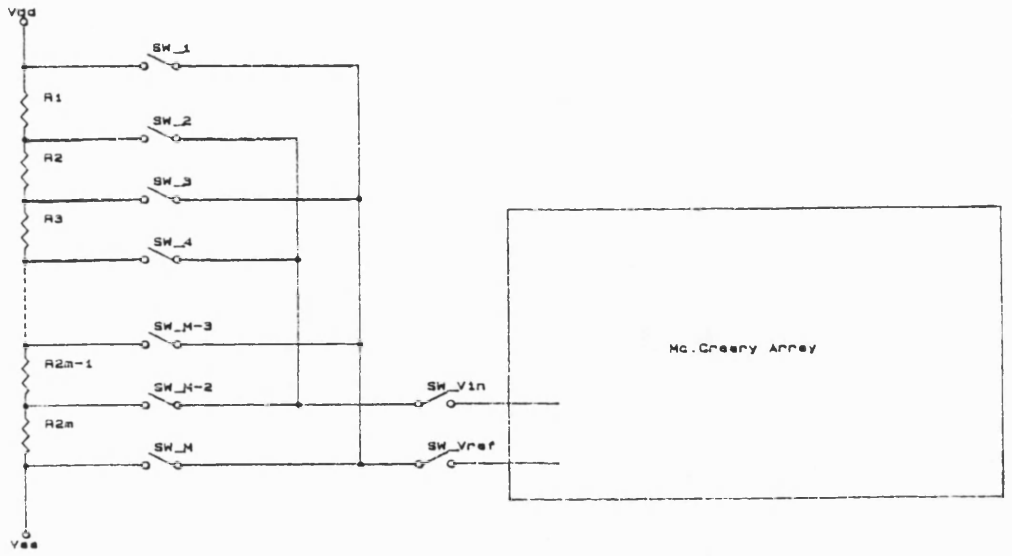


Figure 4.11 Fotohui AD-Converter

The concept is a mixture of the McCreary principle and the Hamadé principle. The resistor string operates with the MSB's. The "McCreary" part of his design does not use the reference voltage for the comparison. The redistribution is done with the resulting voltage of the resistor array after completion of the MSB-part. Therefore the resistor string is a rough quantisation. The exact quantisation is done with the capacitor array, based on the new reference voltage. The advantage of this concept is an increase in the resolution, with the advantages of the McCreary concept combined with the Hamadé concept.

4.8.5 Lee - Hodges Principle

The Lee-Hodges A to D converter was presented on 3rd. March 1983 [6]. Figure 4.12 shows the circuit drawing.

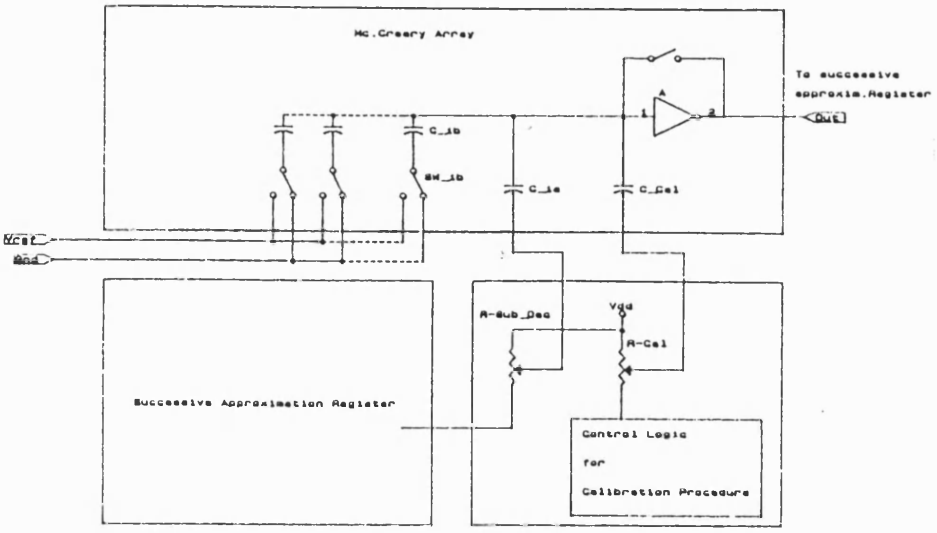


Figure 4.12 Lee-Hodges AD-Converter

This design is a self calibrating switched capacitor A to D converter. The capacitor array is based on the McCreary concept, whereby the less significant bits are converted using a binary weighted resistor string. The matching between the resistor sub-DAC and the capacitor array is first calibrated with an additional calibration DAC first. The self calibration isdone using another additional resistor string. This requires a charge transfer into the calibration capacitor, designed with the same size as the LSB capacitor. This calibration charge depends on the measured error voltage after completion of the calibration cycle. Therefore the calibration voltage shifts the reference level of the comparator. The calibration cycle begins by measuring the nonlinearity due to the MSB capacitor. During the calibration cycle, all the capacitors first have to be connected to V_{ref}, except the MSB capacitor. After completion of the charging of the array, the charge will be redistributed by complementing all the switches viz: all switches to 50% V_{dd}, except the MSB capacitor. The MSB capacitor is connected to V_{ref}. The remaining error charge at the top plate of the array will be measured and cancelled by the calibration DAC charge on the LSB calibration capacitor. This self calibration technique shifts the A to D conversion accuracy into the 14 to 16 bit resolution. This is possible with a sample rate of about 50 kilosample per second.

4.8.6 The Redfern Principle

In December 1979 Redfern published his principle based on a resistor string and a two capacitor array [7]. Figure 4.13 shows the circuit drawing.

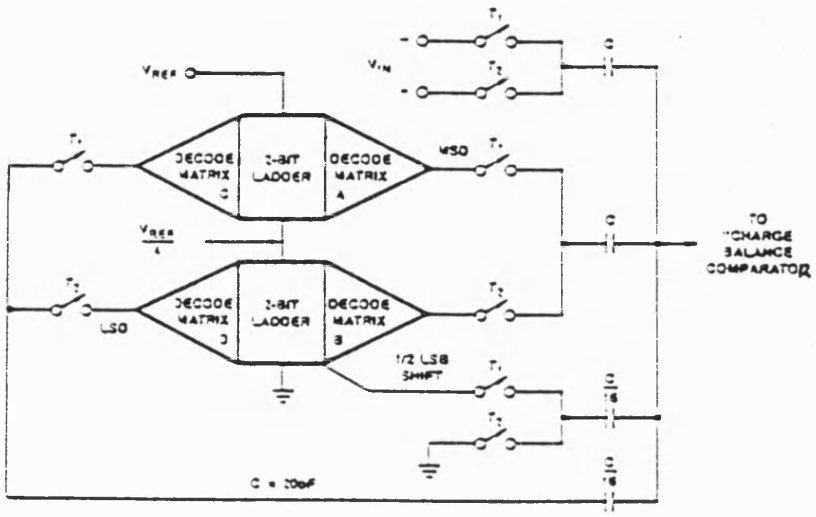


Figure 4.13 Redfern AD-Converter

The input of the comparator is connected to the summing node of this capacitor array. The basic idea is split into two parts:

1. The A to D conversion done using a resistor array divided into two strings :

a. The upper string (near to the reference voltage) is the MSB ladder - the resistors are weighted with an unity " R ".

b. The lower string is the LSB ladder - the resistors are weighted with "R/N" (N = number of bit's). The charge on the LOW ladder will be stored on a weighted capacitor. The capacitor weight used in this concept is balanced for each resistor string.

An additional resistor, which may be used to increase the resolution, needs a new pair of capacitors, weighted to the reduction factor of the reference used in the new R-string. Figure 4.14 shows a 13 bit Redfern AD-converter [7].

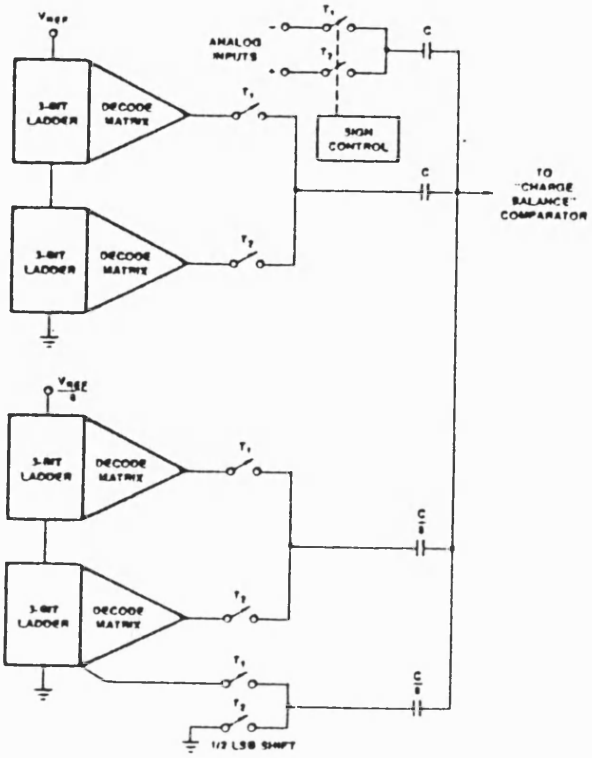


Figure 4.14 13 Bit Redfern AD-Converter

2. Charge balancing of the comparator circuit: The charge balancing starts with the initialisation of the comparator. The resistor string is connected via a switch to the MSB. The other capacitor is connected to the positive input voltage. The next cycle activates the comparator, with the resistor switch changing from the MSB connection to the LSB connection. The voltage drop of the resistor array at the bottom plate of the capacitor is therefore 1/2 V_{ref}. Within this cycle, the bottom plate of the second capacitor is switched to the inverse input voltage. The decision of the comparator depends on the situation: if the voltage change of the input voltage ΔV_{inp} is bigger than the change of the related binary weighted reference voltage ΔV_{ref}, the comparator flags a "LOW" output and the MSB is "1". The next cycle starts with the same MSB

connection, if the decision of the previous cycle was MSB = 1. Otherwise, the MSB will be connected to the related lowest node. The resulting output drop at the resistor array is 0.75 V_{ref} (MSB = 1) or 0.25 V_{ref} (MSB = 0). The capacitors used in this circuit are weighted to 1 for the input voltage, as well as for the MSB conversion ladder. The LSB conversion ladder has capacitors weighted as explained above. This weight can be increased when the reference voltage is decreased. Increasing the LSB weight will be applicable for higher resolution ADC, due to mismatch of capacitors. To obtain high accuracy with this technique, laser trimming of the resistor array is required.

4.8.7 The Li - Principle

In August 1986, Li published his A to D converter based on the reference refreshing cycling principle [9,10]. Figure 4.15 shows the circuit diagram.

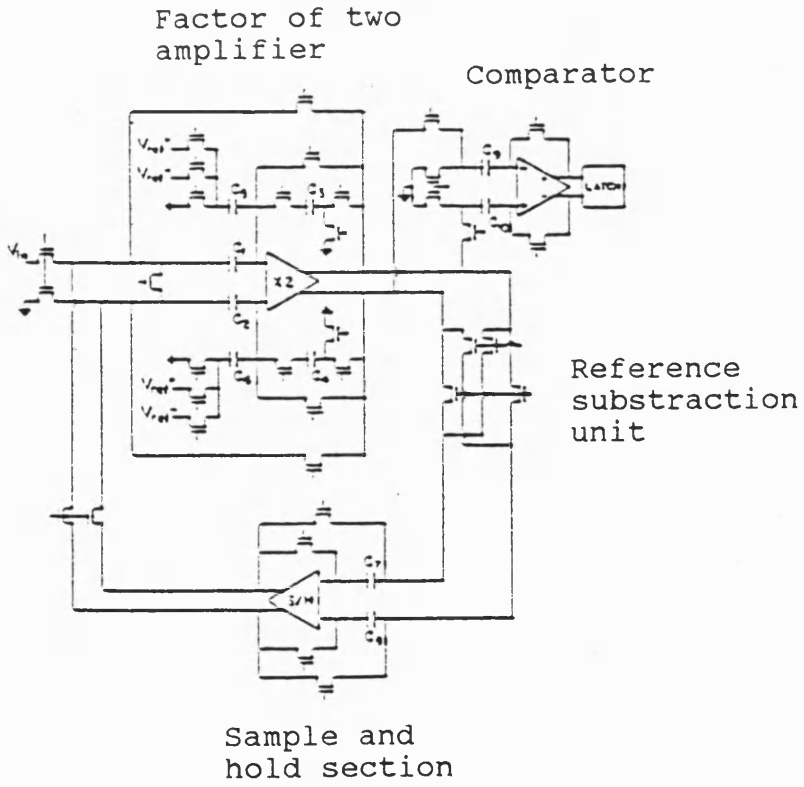


Figure 4.15 Li AD-Converter

This is an advanced algorithmic principle. The first realization of a cycling A to D converter principle was introduced by Hornak in February 1975 [16]. The basic components of reference cycling converters are :

a. The sample and hold section,
b. The factor of two amplifier,
c. The comparator,
d. The reference subtraction unit.

If the signal is in the lower plane, the input signal will be doubled and the MSB set to "0". The MSB is forced high when the signal is in the upper plane. The reference voltage, which is 50% supply voltage is subtracted from the input voltage. During the next cycle the remainder of the previous cycle is used as the new input voltage. The comparison process is repeated. N bit A-D converters need N iteration intervals. The reference refreshing principle is a modification of the cyclic concept. To avoid inaccuracies during analogue to digital conversion, the reference voltage must be handled in comparison to the input signal. The input signal is sampled before the first conversion process starts. Within the standard cyclic concept, the reference voltage is loaded at the beginning of each A-D cycle. The advantage of the reference refreshing A-D principle is the sampling of the reference voltage. The following bit by bit conversion cycles take the reference voltage cycling around like the signal. Therefore the error voltage of the reference voltage is:

$$V_{ref,n} = V_{ref,0} \cdot \left(1 + \frac{E_1}{2}\right)^n \tag{4.31}$$

The term E_1 here is the first order error voltage of the reference voltage. All the higher order error voltages will be reduced with this principle as well.

4.8.8 The Delta Sigma Principle

Goodman [12] and Greenstein [17] proposed the delta modulation in 1969 and 1973, respectively, operating at a clockrate many times faster than the Nyquist frequency of the signal bandwidth. Figure 4.16 shows the circuit diagram.

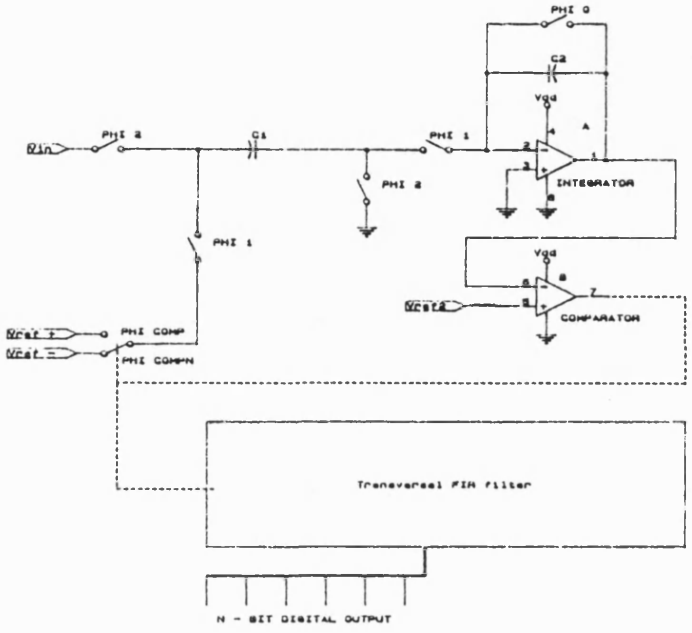


Figure 4.16 Delta Sigma AD-Converter

The Delta Sigma principle has the advantage that it fulfils high demands of both linearity and a large baseband (about 50 KHz using standard processes is achievable). These requirements normally need a laser trimmed array technique or a self calibrating principle.

Following the first proposal published by Goodman and Greenstein, lots of publications of oversampled A to D converters acting either with a linear predictive, or a noise - shaping code concept, enabled the delta principle to be a standard procedure [18,12-14]. The sigma part of this converter approach consists of the summation of the input signal and the delta quantum, that is the correction term. At the end of the sample period, this quantum toggles from step to step. All of the samples taken during one

conversion period will be summed in a digital register and at the end of the conversion, they will be divided by the total number of samples. Hence this statistic - a Gaussian distribution - gives an averaging of values detected during each A to D conversion. This 1 bit A to D procedure is oversampled, that means the sample frequency is beyond the Nyquist limit of the baseband. The oversampling technique distributes the quantisation noise over the frequency range from DC to the Nyquist frequency of the sample clock. A noise shaping technique (low pass filtering) is used to shift most of the noise beyond the upper baseband limit. The correction term control is fed back via a 1 bit DAC. Dependent on the decision of the comparator a correction voltage is added or subtracted at the summation node. The output signal of a Delta Sigma AD converter is a high speed 1 bit data train. This data train must be collected and digitally filtered. The digital filtering needs a higher order filter term than the noise shaping function. The digital filter is a low pass filter to remove the high-frequency noise from the signal. Decimation techniques of digital filtering are often in use to reduce the data rate to lower frequencies.

A periodic stream of zeroes and ones with a toggle frequency of exactly half the clock frequency is achieved with an ideal ADC (i.e. no offset voltage, and the input voltage at midpoint of full range). Small DC values at the input result in additional zeroes or ones in the data train. The appropriate Fourier spectrum shows discrete lines at about DC, Nyquist frequency, sample frequency and so forth. This effect is well known in Delta Sigma converters, especially of the first order. Minimizing this effect can be achieved using a dithering circuit [11].

In a later chapter a new delta sigma principle will be presented in which the integration of the data is put into the digital part. This enables this A to D converter to operate in an oversampled mode, or to operate as an A to D converter on random signals but with a lower (12 bit) resolution.

4.9 Summary of the AD Principles

AD-Principle	Accuracy	Speed	Limitations
McCreary	8-10 bit	0.5-5 MHz	Vref, Cmat, cft
Suàrez	4-6 bit	0.5-5 MHz	Cp, Vref, Cmat, cft
Hamadé	8 bit	10-100 KHz	Rmat, RT, Vref
Fotohui	10-12 bit	10-100 KHz	Vref, Cmat, cft, Rmat, RT
Lee-Hodges	12-15 bit	10-100 KHz	Vref, cft, Cmat
Redfern	8-12 bit	0.1-1 MHz	Vref, cft, Cmat, Rmat, RT
Li	12-13 bit	10 KHz	Vref, Cmat, cft
Delta Sigma	12-14 bit	signal: 50 KHz clock: 5 MHz	Vref, Cmat, cft

Cp : parasitic capacitors

cft : clock feed through

Cmat : capacitor matching

Rmat : resistor matching

RT : resistor laser trim

com : component mismatching

Vref : reference stability

4.10 Advanced A to D Techniques

Factors contributing to the limitation of the accuracy [most influence on the accuracy limitation] include the stability of the reference voltage, the influence of the parasitic capacitors and the clock feed through error voltage. Advanced A to D principles should minimise most of these factors. Minimising these effects needs components with enhanced accuracy (see Chap. 3) and new design techniques. In Chapter 5 new principles to stabilize the reference voltage, based on charge conservation techniques using voltage inverter switches (VIS), will be presented. Some different VIS circuits are theoretically discussed, simulated and built on PCB. Chapter 7 introduces six new A to D circuits:

1. A VIS controlled Suàrez converter with a much increased resolution.
2. An algorithmic ADC.
3. A difference Sigma Delta ADC (SD-ADC).
4. An incremental VIS controlled SD-ADC.
5. An incremental fully differential D-VIS controlled SD-ADC.
6. A fully differential D-VIS controoled SD-ADC.

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C H A P T E R 5

5. VIS Principles

5.1 Introduction

As discussed in section 4.17, the accuracy of ADC references can be improved by using the voltage inverter switch (VIS) principle. This chapter presents novel reference sources for the use in A to D converters based on VIS circuit techniques. The VIS principle was first presented by Fettweis in 1979 [1,2] and has been used in many analogue filter designs [3-7]. VIS circuits have the advantage that special circuit elements such as coils, transformers, gyrators and unit elements can be designed using switched capacitors. These elements are in common use in discrete designed filter applications of higher orders.

The advantage of the VIS principle is that it may be regarded as lossless as a result of the following two steps:

Step 1: Measurement of the nodal voltages before the charge transfer begins.

Step 2: Completion of the charge transfer by incorporating an additional charge, in order to fulfil the condition that the energy before step 2 is equivalent the energy after completion of step 2.

5.2 Basic VIS Circuit Operation

Figure 5.1 shows the basic switched capacitor circuit.

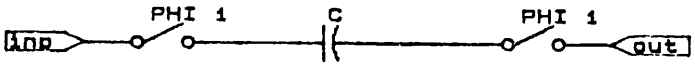

Figure 5.1 A Switched Capacitor

The capacitor C is periodically charged, the amount of charge is being quantized. With the index definitions

a = after the switched event

b = before the switched event

the voltage at the end of a period in which both switches are closed is:

$$Va(tn) = Vb(tn) + \frac{q(tn)}{C} \tag{5.1}$$

Assuming no discharge is detected during switch opening time, the voltage directly before the switches close is given as:

$$Vb(tn + 1) = Va(tn) \tag{5.2a}$$

or in the z-domain

$$z \cdot Vb = Va \tag{5.2b}$$

The equilibrium voltage of a switched capacitor over one period of time is:

$$V(tn) = \frac{Va(tn) + Vb(tn)}{2} \tag{5.3}$$

In the steady state, the appropriate voltages and charge can be described by:

$$va(tn) = Va \cdot e^{ptn}$$
$$vb(tn) = Vb \cdot e^{ptn}$$
$$v(tn) = V \cdot e^{ptn}$$
$$q(tn) = Q \cdot e^{ptn}$$
$$Q = C \cdot (Va - Vb) \tag{5.4}$$

where:

Va, Vb, V and Q are complex numbers. Arrangement of the equations above results in:

inserting $vb(tn) = va(tn + 1) \cdot e^{ptn}$ and eqn (5.3) in eqn (5.4) gives:

$$V = \frac{Q}{2 \cdot C} \cdot \frac{1 + e^{-pT}}{1 - e^{-pT}} \tag{5.5}$$

to simplify further, V(tn) is abbreviated with V

$$Q = I \cdot T$$

$$V = \frac{T}{2 \cdot C} \cdot \frac{Va + Vb}{Va - Vb} \cdot I \tag{5.6}$$

$$\frac{Va + Vb}{Va - Vb} = \frac{1}{\Psi}$$

Following Maxwell [8], the term T/2C has the dimensions of resistance. Therefore eqn.(5.6) can be rewritten as

$$V = \frac{R}{\psi} \cdot I \tag{5.7}$$

Eqn.(5.7) describes the identity of a switched capacitor and an ohmic resistor within the ψ-plane. Inversion of the voltage over the capacitor, directly after the switches have opened, results in:

$$Vb(tn+1) = -Va(tn) \tag{5.8}$$

The set of equations that describes the voltage inversion is given by:

$$Va(tn) = -Vb(tn) + \frac{q(tn)}{C} \tag{5.9}$$

$$V(tn) = \frac{Va(tn) + Vb(tn)}{2}$$

$$V = \frac{T}{2C} \cdot \frac{Va + Vb}{Va - Vb} \cdot I = \frac{R \cdot I}{\psi} \tag{5.10}$$

where:

$$\psi = \tan h\left(\frac{pT}{2}\right) = \frac{1 - e^{-pT}}{1 + e^{-pT}}$$

The time domain description of eqn.(5.10) is a capacitance. Complete discharge of this capacitor before each charge cycle results in the description of an ohmic resistor:

$$V = \frac{1}{2C} \cdot \frac{Va}{Vb} \cdot Q = R \cdot I \tag{5.11}$$

Equivalent procedures transform a voltage source with an internal ohmic resistor and so forth into its appropriate SC-circuit.

Table 5.1 shows the most important equivalent devices.

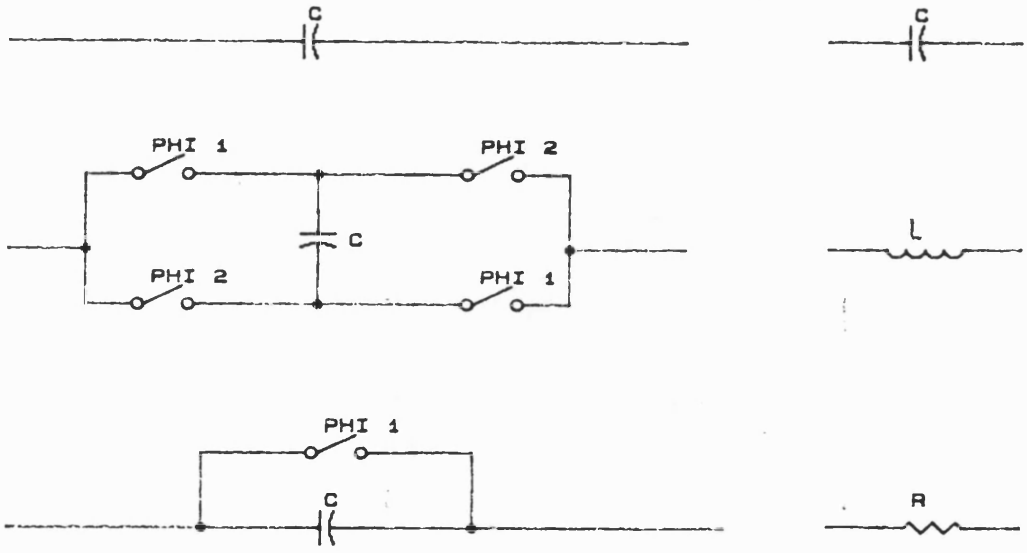

Table 5.1

The accuracy of SC-circuits is dependent on the charge splitting between the network elements including their parasitics. Improvement in charge distribution between two capacitors can be achieved, if the losses produced by the components can

be minimized. An element that fulfils this requirement is a voltage inverter switch (VIS).

The operation of a VIS circuit is shown in figure 5.2.

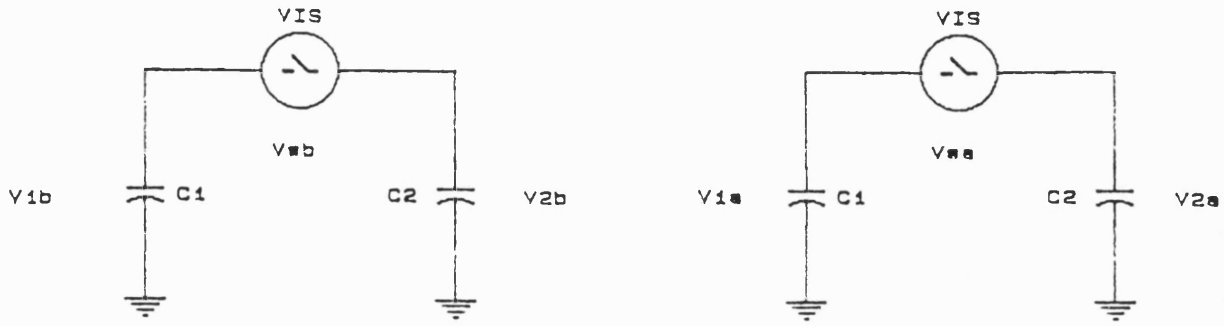

Figure 5.2 Basic operation of a VIS

The energy stored in C1 is completed distributed over C1 and C2 after completion of a VIS cycle.

The energy Wsb before the charge distribution is given as:

$$Wsb = \frac{1}{2} \cdot \frac{C1 \cdot C2}{C1 + C2} \cdot (Vsb)^2 \qquad (5.12)$$

After completion the VIS cycle, the energy stored in both capacitors is:

$$Wsa = \frac{1}{2} \cdot \frac{C1 \cdot C2}{C1 + C2} \cdot (Vsa)^2 \qquad (5.13)$$

Hence the lossless charge transfer results in

$$Wsb = Wsa \tag{5.14}$$

Equation (5.14) has two solutions.

$$Vsb = Vsa \tag{5.15a}$$

$$Vsb = -Vsa \tag{5.15b}$$

Solution (5.15b) is of particular interest. This eqn. describes the voltage inversion process. The total charge transfer of a VIS cycle can be described as:

$$q_{VI} = 2 \cdot \frac{C1 \cdot C2}{C1 + C2} \cdot Vsb \tag{5.16}$$

This charge is twice that flowing through a standard switch.

5.3 Nonidealities

It is well known, that the charging of capacitors within an integrated circuit results in leakage charges flowing through the parasitics of the circuit [9,10]. Therefore the KCL is not valid for the signal path. Nonidealities can be described with a correction factor α.

$$Va = -\alpha Vb \tag{5.17}$$

Other influences that limit the accuracy are finite gain of the active elements, mismatching of devices and non linearities of the transfer-gates. These items are discussed in sections 5.5, 5.6 and 5.7, where the different VIS principles are presented.

5.4 VIS Principles

It is obvious that to monitor the charge distribution a detector that monitors the error charges is required. Two VIS principles which monitor the charge flow during the distribution phase have been proposed: the floating and the grounded VIS circuit (Figure 5.3).

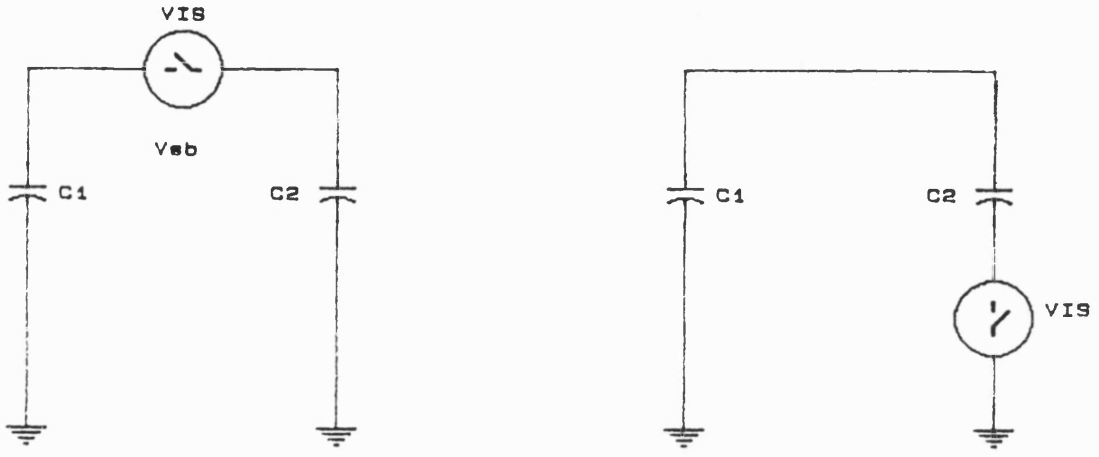

Figure 5.3 Floating and Grounded VIS

Based on experience [3,4,5,9], the grounded VIS principle exhibits less sensitivity to stray capacitances.

The following VIS principles will be examined in the following sections.

- Voltage follower VIS (V-VIS)
- Integrator VIS (I-VIS)
- VIS based on differential amplifier design (D-VIS)

5.5 The Voltage Follower VIS Principle (V-VIS)

5.5.1 Voltage Follower VIS Type 1

Figure 5.4 shows the circuit drawing of a V-VIS presented by Herbst in 1981 [3]. The V-VIS operates in three basic phases.

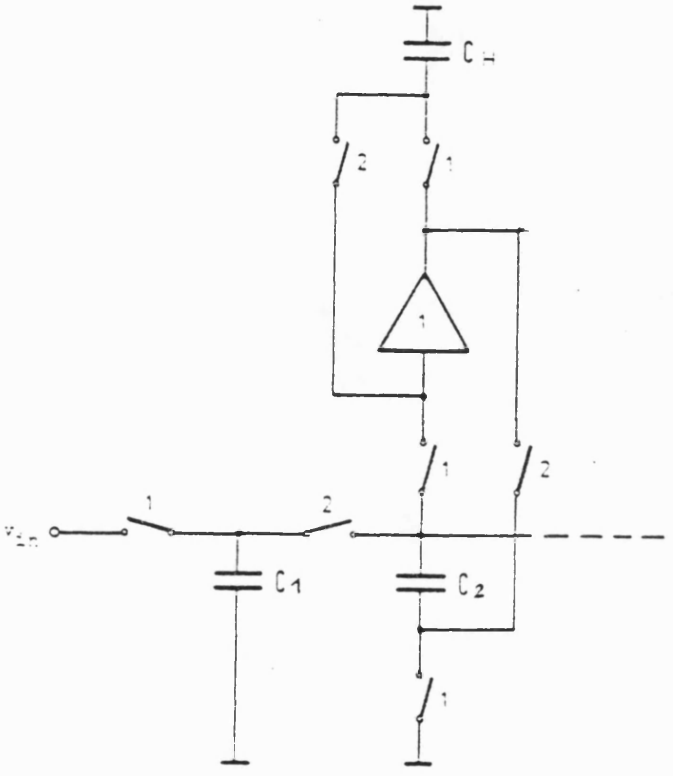

Figure 5.4 Voltage Follower VIS Circuit

Phase 1: All switches with index 1 are closed (all other switches open). This prepares the system offset (i.e. amplifier offset and clock feed through offset) which will be canceled in the next phase.

Phase 2: All switches with index 2 are closed. The charge stored in C1 will be redistributed with C2 and additionally the overall error correction charge produced by the V-VIS is stored in the capacitor array.

This procedure will now be described in detail. The charge flow during the charge redistribution phase is given by:

$$q = \frac{C1 \cdot C2}{C1 + C2} \cdot (V_1 b - 2V_2 b) \tag{5.18}$$

The voltage across capacitor C2 at the end of phase 2 is:

$$V_2 a = V_2 b + \frac{C1}{C1 + C2} \cdot (V_1 b - V_2 b) \tag{5.19}$$

where:

V_1b: the voltage across C1 at the end of phase 1

V_2b: the voltage across C2 at the beginning of phase 2

It can be seen in eqn.(5.19) that the overall offset compensation term (V_2b) is included by the VIS-loop during phase 2. In A to D converter circuits, the charge sharing coefficient is most often 2, so both capacitors should have the same value. Equivalent capacitors should have equivalent parasitic capacitances, and from the circuit design, their parasitic effect is canceled. However, secondary effects such as variation in oxide thickness may result in unbalanced parasitics. In order to minimize these effects the capacitors C2 and C1 should be laid out using unity capacitance structures within a hard-grounded p-well. The value of the auxiliary capacitor C_H, used

to store the offset voltage, is dependent both on the stability of the amplifier and the charge sharing characteristic between C_H and the effective input capacitance of the amplifier, C_{in}. The charge redistribution between C_H and C_{in} during phase 2 is given by eqn.(5.20).

$$q_{CH} = \frac{C_H \cdot C_{inp,eff}}{C_H + C_{inp,eff}} \cdot (V_{CH} - V_{Cinpb}) \qquad (5.20)$$

where:

V_{CH}: is the voltage across C_H at the beginning of phase 2

VC_{inpb}: is the voltage across the amplifier input capacitance at the beginning of phase 2

From eqn.(5.20), the voltage across C_{inp} at the end of the charge distribution is given by:

$$V_{Cinp}a = \frac{q_{CH} - q_{Cinp,eff}}{C_{inp,eff}} = \frac{C_H}{C_H + C_{inp,eff}} \cdot (V_{CH} - V_{Cinpb}) \qquad (5.21$$

where:

q_{CH} is the charge on C_H at the start of the redistribution phase

The voltage V_{Ciupb} consists mainly of the remaining offset error of the chopper OTA, the clock feed-through error voltage induced by the transfer-gates and an error voltage term induced by ringing of the supply lines. An error term α_1 can be defined as:

$$\alpha_1 = \frac{q_{CH} - q_{Cinp,eff}}{q_{Cinp,eff}}$$

$$\alpha_1 = \frac{q_{CH}}{q_{cinp,eff}} \cdot (1 - \frac{C_{inp,eff}}{C_{II} + C_{inp,eff}} \cdot (1 + \frac{V_{Cinpb}}{V_{CII}})) \tag{5.22}$$

$$\alpha_1 = \frac{q_{CH} \cdot \beta}{q_{Cinp,eff}}$$

A second term, α_2 that contributes to the internal VIS error is the limitation of the amplification. The maximum accuracy achievable with this amplifier concept is proportional to 1/A0. Hence α_2 can be defined as:

$$Va = -Vb(1 + \alpha_1) \cdot \left(1 + \frac{1}{A0}\right)$$

$$\alpha_2 = 1 + \frac{1}{A0} \tag{5.23}$$

Eqn.(5.17) can now be rearranged with eqn.(5.22) and (5.23):

$$Va = Vb \cdot (1 + \alpha_1) \cdot \alpha_b \tag{5.24}$$

The signal voltage swing using a V-VIS concept is limited by the internal voltages of the amplifier and can be described as:

$$V_{SS} + V_\tau =< V_{inp} =< V_{DD} - V_\tau \tag{5.25}$$

5.5.2 Voltage Follower VIS Reference Circuit Type 1

Figure 5.5 shows the V-VIS A to D reference circuit. During phase 0, the input capacitor is charged to V_{DD}. Phase 1 and 2 are the measurement and voltage inverter phase respectively. The phase 3 is used to transform the signal to a low impedance reference output by using the same amplifier. Phase 4 is used to discharge the capacitor C1 to prepare the V-VIS for the next cycle.

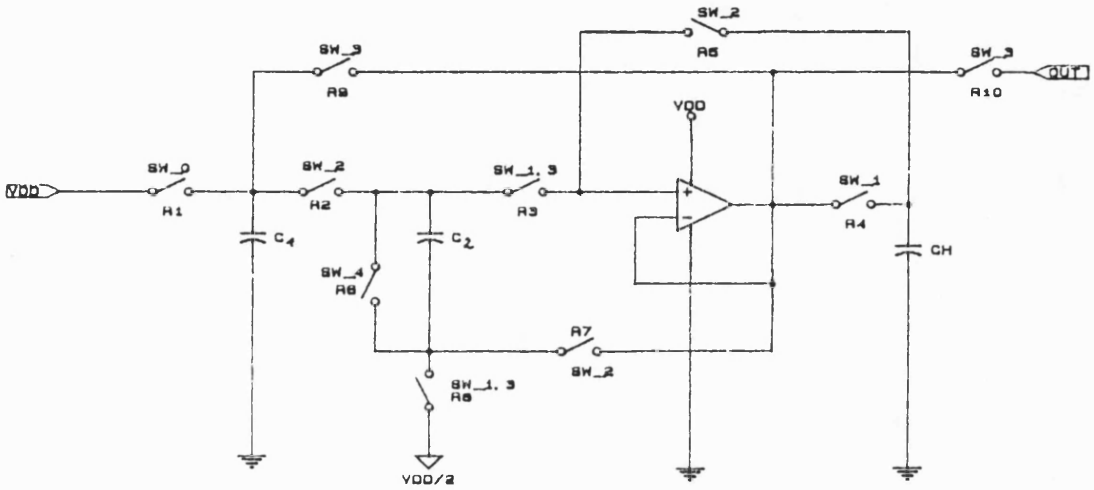

Figure 5.5 V-VIS A to D Reference Circuit

Inspite of the explained operation phases of fig. 5.4, the V-VIS reference circuit needs an additional phase:

Phase 3: All switches with index 3 are closed. The voltage across C2 gives the low impedance value for use in the following stages.

5.5.3 Voltage Follower VIS Reference Type 2

Other V-VIS design concepts have been presented by Herbst [3]. These concepts can be easily adapted for use in an A to D reference circuit. Figure 5.6 shows a

modified V-VIS circuit. During phase 1 the differential voltage between node 10 and node 20 is stored on the auxiliary capacitor C_H. The top plate of C_H is connected in phase 2 to the input of the second voltage follower EVIS2, while the bottom plate is hard connected to signal ground. Therefore the output voltage of EVIS2 can be written as:

$$V_{out,EVIS2} = -(V_1 b - V_2 b) \tag{5.26}$$

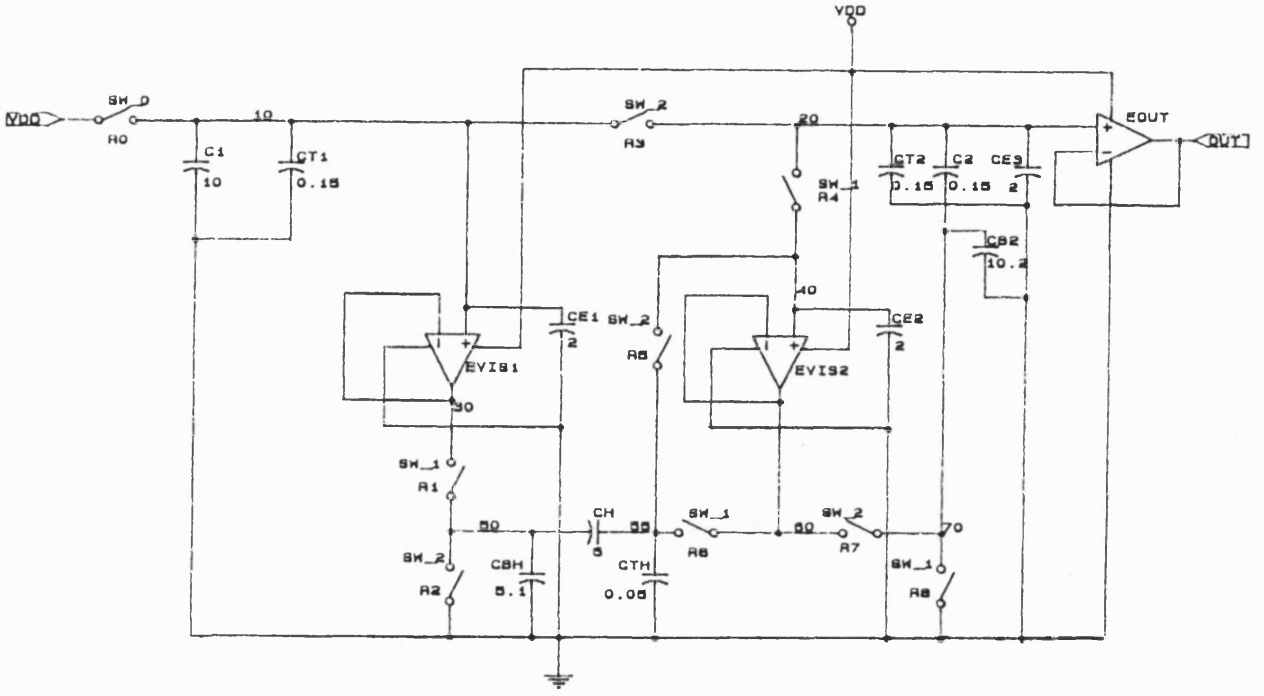

Figure 5.6 Modified Voltage Follower VIS A to D Reference Circuit

Herbst showed that this concept is not lossless, because of the influence of the input capacitance of the voltage follower 2 (EVIS2) and the additional influence of the parasitic capacitances C_{T1} and C_{T2}, which are not cancelled.

Other voltage follower concepts [4,5] show the same criteria. Hence the V-VIS

circuit presented in section 5.5.1 is the best principle to use as an A to D reference circuit, because of its internal stability against parasitic capacitances. The only disadvantage is a limitation of the input voltage.

5.6 The Integrator VIS (I-VIS)

The Integrator VIS principle has the best performance for a VIS circuit [1-6], because of the accuracy that can be achieved using an SC-integrator characteristic. Figure 5.7 shows the circuit diagram of an I-VIS concept to be used in A to D converters.

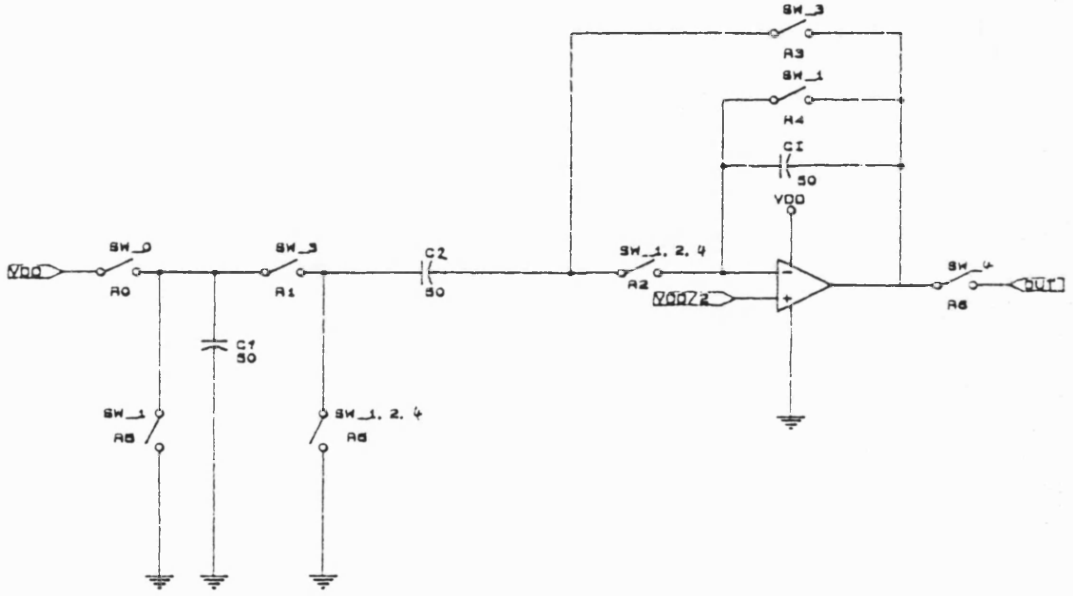

Figure 5.7 I-VIS A to D reference

The circuit operation needs 4 different clock phases.

Phase 1: Offset cancelling for the amplifier

Phase 2: Cancelling the clock feed through of the switches and measurement of the signal ground potential.

Phase 3: Voltage inversion of the error potential to signal ground measured during phases 1 and 2 and charge distribution between C1 and C2.

Phase 4: The voltage across C2, which is identical to the voltage across C1, is now outputted.

This procedure can be described as:

Phase_1

At the start of each cycle, the voltage across C1 is

$$V_{C1} = V_{ref} \cdot (Beginning \quad of \quad ADC - cycle)$$

where V_{ref} is the reference voltage for that particular cycle. At the start of the nth cycle, the voltage across C1 is

$$V_{C1} = V_{n-1} \cdot (n - th \quad ADC - cycle)$$

The voltage across C2 in this phase is the remaining offset of the chopper operational transconductance amplifier (OTA), V_{off}.

$$V_{C2} = V_{off}$$

where V_{off} is given by

$$V_{off} = \frac{V_{DD} + V_{SS}}{2} + V_{offOTA}$$

$V_{off\,OTA}$ is the inherent offset voltage of the OTA. We also have in this phase

$$V_{CT2} = 0$$

$$V_I = 0$$

$$V_{out} = V_{off}$$

where the subscipts CT1,2 refer to the top plate parasitics of C1,2 respectively, and V_{C1} is the voltage across the integration capacitor C1.

Phase_2

The output voltage from the integrator circuit is given by

$$V_{out} = -\frac{C2}{C_I} \cdot (V_{inp} + V_{off} + V_{CfT,R2})$$

where $V_{cf,R2}$ is the clock feed through voltage induced by switch 2. If we have C2 = C_I:

$$V_{out} = -(V_{inp} + V_{off} + V_{CfT,R2})$$

where:

$$V_{off} = \frac{V_{DD} + V_{SS}}{2} + V_{off\ OTA}$$

Phase_3

The redistribution charge, q_3 is given by

$$q_3 = \frac{(C1 + CT1) \cdot (C2 + CT2)}{C1 + CT1 + C2 + CT2} \cdot (V_{C1}b - V_{C2}b) \tag{5.27}$$

$$V_{C2}b = V_{CfT,R3} - V_{off} - V_{Cft,R2} \tag{5.28}$$

where $V_{Cft,R2,3}$ is the clock feed through of switch R2 and R3 respectively.

If the transfer-gates have identical geometries, the clock feed through voltages should be identical and eqn. (5.28) can be simplified to:

$$V_{C2}b = -V_{off} \tag{5.29}$$

Eqn (5.27) can now be solved to examine the voltage across C1 after redistribution and by neglecting V_{C2b}, since V_{off} is negligible when using chopper amplifiers.

$$V_{C1}a = \frac{C2 + CT2}{C1 + CT1 + C2 + CT2} \cdot V_{C1}b$$

where $V_{C1}a$ is the voltage across C1 after completion the charge redistribution. Using balanced capacitances such that C2=C1=C, and CT1=CT2=CT, then

$$V_{C1}a = \frac{C+CT}{2C+2CT} \cdot V_{ab} = \frac{C+CT}{2(C+CT)} \cdot V_{C1}b$$

$$V_{C1}a = \frac{1}{2} \cdot V_{C1}b \qquad (5.30)$$

Equation (5.30) shows the perfect divide-by-2 operation that will be required for the novel ADC reference circuits. Since traditionally, clocked circuits are described using the z-transform, we shall examine the operation of this circuit, starting in the time domain, to derive the transfer function in this form. Note that the valid output voltage is only available during the clock phase 4.

$$V_{out}(t_0+nT) = V_{inp} \cdot (n \cdot T) \quad + \quad \left(\frac{C1 \cdot C2}{C1+C2}\right) \quad \cdot \quad \frac{q_3}{C2} \qquad Phase \quad 3 \qquad (5.31)$$

$$V_{out}(t_0+nT) = V_{out} \cdot (t+(n-1) \cdot T) - \frac{C}{C_I} \cdot V_{inp} \cdot (t+(n-1) \cdot T) \quad Phase \quad 4 \qquad (5.32)$$

where:

T = period time

t_0 = time within T, at which the voltage is valid

V_{inp} = constant during the measurement phase

To analyse eqn (5.31) in the frequency domain, a sample train is required. In order to simplify this procedure, the sample train used is a Dirac comb function given by:

$$\delta(t) = \sum \delta \cdot (t-nT) \qquad (5.33)$$

Using a rectangular signal rect (t/T) gives:

$$F(j\omega) = si \cdot \left(-\frac{\omega T}{2}\right) \cdot \sum_{n=-\infty}^{n=\infty} F(j\omega - jn\omega_0) \tag{5.34}$$

where:

ω_0 is the fundamental frequency by using the rectangle signal related to the duration of the rectangular signal

where: $si(x) = \frac{\sin x}{x}$

$$\sum_{n=-\infty}^{n=\infty} V_{out} \cdot (t_0 + nT) \cdot \delta \cdot (t - t_0 - nT) =$$

$$\sum_{n=-\infty}^{n=\infty} V_{out} \cdot (t_0 + (n-1) \cdot T) \cdot \delta \cdot (t - t_0 - nT)$$

$$-\frac{C}{C_1} \cdot \sum_{n=-\infty}^{n=\infty} V_{inp} \cdot (t_0 + (n-1) \cdot T) \cdot \delta \cdot (t - t_0 - nT) \tag{5.35}$$

To convert this signal to the frequency domain, we perform the Fourier transform.

$$F(\sum_{n=-\infty}^{n=\infty} V_{out} \cdot (t_0 + nT) \cdot \delta \cdot (t - t_0 - nT) =$$

$$\sum_{n=-\infty}^{n=\infty} \int_{t=-\infty}^{t=\infty} V_{out} \cdot (t_0 + nT) \cdot \delta(t - t_0 - nT) \cdot e^{-pT} dt =$$

$$\sum_{n=-\infty}^{n=\infty} V_{out} \cdot (t_0 + nT) \cdot e^{-p\left(t_0 + nT\right)} \cdot \int_{t=-\infty}^{t=\infty} \delta(t - t_0 - nT) dt =$$

$$\sum_{n=-\infty}^{n=\infty} V_{out} \cdot (t_0 + nT) \cdot e^{-pt_0} \cdot e^{-npT} =$$

$$\sum_{n=-\infty}^{n=\infty} V_{out} \cdot (t_0 + nT) \cdot z^{-n} \tag{5.36}$$

where $p = j\omega$

It can be seen from eqn (5.36) that the Fourier transform of the input voltage is given by

$$V_{inp}(z) = \sum_{n=-\infty}^{n=\infty} V_{inp} \cdot (t + nT) \cdot z^{-n} \tag{5.37}$$

From eqn.(5.35) the output voltage can be written as:

$$V_{out}(z) = V_{out}(z) \cdot z^{-1} - \frac{C}{C_I} \cdot V_{inp}(z) \cdot z^{-1} \tag{5.38}$$

$$V_{out}(z) = -\frac{1}{1 - z^{-1}} \cdot \frac{C}{C_I} \cdot V_{inp}(z) \cdot z^{-1} \tag{5.39}$$

Therefore the transfer function is defined as:

$$H(z) = \frac{V_{out}(z)}{V_{inp}(z)} = -\frac{C}{C_I} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{5.40}$$

Another arrangement of eqn (5.40) that is often used is:

$$H(p) = -\frac{C}{C_I} \cdot \frac{1 - pT}{pT} \tag{5.41}$$

5.7 The Differential Controlled VIS

Following the design principles of the integrator VIS circuit, an additional improvement can be achieved by using a fully symmetric concept. Based on the fully symmetric OTA [11], the differential controlled VIS (D-VIS), shown in figure 5.8 was developed. This D-VIS circuit was firstly presented by Montecci [7] and is here rearranged for the use as an A to D reference. Figure 5.8 shows the circuit diagram of a D-VIS.

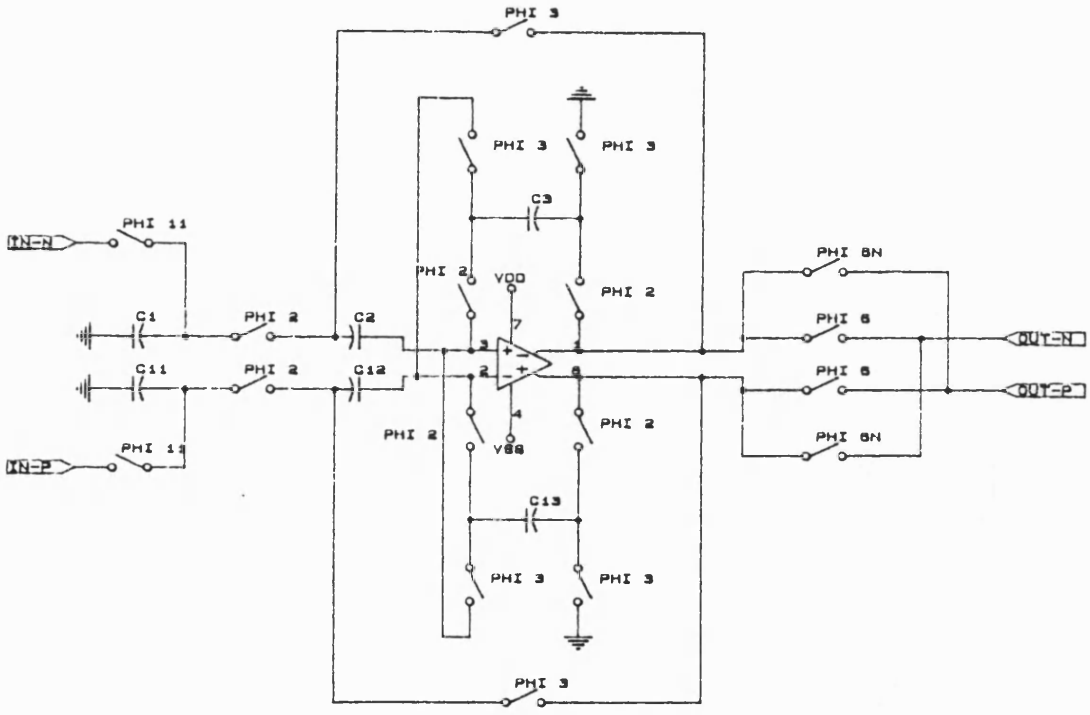

Figure 5.8 Fully Differential VIS A to D reference circuit

The output voltages V_i + and V_i - are given as:

where i is b before, and a for after charge redistribution

$$Vb_+ = -Vb_- = \frac{1}{2}\left(\frac{q_{b-}}{C13} - \frac{q_{b+}}{C3}\right) \tag{5.42}$$

After completion of the voltage inversion process, the output voltages are changed to:

$$Va_{+} = Vb_{+} + \frac{q_{b+}}{C1} - \frac{q_{b-}}{C11} + \frac{C13}{C12} \cdot \Delta Vx \tag{5.43}$$

$$Va_{-} = Vb_{-} + \frac{q_{b-}}{C2} - \frac{q_{b+}}{C12} + \frac{C3}{C2} \cdot \Delta Vx \tag{5.44}$$

$$\Delta Vx = (q_{b+} - q_{b-}) \cdot \left(\frac{1}{C2} - \frac{1}{C1} \right) \cdot \left(\frac{C3}{C2} + \frac{C13}{C12} + 2 \right)^{-1} \tag{5.45}$$

Using the equations (5.43 - 5.45) to derive the differential output voltage after completion the VIS cycle (phase 3) gives:

$$(Va_{+} - Va_{-}) = (Vb_{+} - Vb_{-}) + q_{b+} \cdot \left(\frac{1}{C1} + \frac{1}{C2} \right) - q_{b-} \cdot \left(\frac{1}{C2} + \frac{1}{C11} \right) + \Delta Vx \cdot \left(\frac{C13}{C12} - \frac{C3}{C2} \right) \tag{5.46}$$

Eqn. (5.46) can be simplified by using the fact that the capacitors are balanced so that:

$$\frac{C13}{C12} = \frac{C3}{C2}$$

$C1 = C11 \qquad C2 = C12$

therefore:

$$(Va_+ - Va_-) = (Vb_+ - Vb_-) + (q_{b+} - q_{b-}) \cdot \left(\frac{C1 + C2}{C1 \cdot C2} \right) \tag{5.47}$$

if we have C1 = C2 = C, then

$$(Va_+ - Va_-) = (Vb_+ - Vb_-) + \frac{2}{C} \cdot (q_{b+} - q_{b-}) \tag{5.48}$$

Equation (5.48) shows that the input capacitance is charged by twice the error charge throughout one VIS cycle. Hence during the charge distribution of the active phase (phase 3), the error voltage charge will be subtracted and therefore the system error is minimized.

REFERENCES CHAPTER 5

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C H A P T E R 6

6. Simulation Techniques and Results

A number of software packages have been developed and used in this work for simulation of novel circuits and processing of results. These include:

BONSAI	- main simulation tool (IBM - version)
SC	- specific switched capacitor circuit simulator
MURF	- multi-radix FFT program to convert time domain data into frequency domain
TPLOT	- a graphic post processor for plotting results from the other packages

These packages and their use will now be described in more detail.

6.1 Description of BONSAI

Bosch Network Simulation and Analysis Instrument -BONSAI- has been developed in response to the demand for a simulation package which has very stable characteristics when simulating CMOS analogue designs [1].

A network description file is used as input. Subcircuits, created as stand alone files, may be referenced by this file, and thus included into the description. Two different circuit description levels may be used, "control-source-level", and the "transistor-level". After simulation two files are produced:

1. .BO file : the ASCII output file.
2. .SXX file(s) : the binary file(s).

The binary file(s) can be read by a graphic post processor like TPLOT. TPLOT reads the binary files produced by BONSAI, MURF or SC and arranges the graphic pictures on the screen. An HPGL-interface to drive an HP-7475A plotter is also included. There are some mathematical options programmed to order a linear regression analysis or to combine curves mathematically. The last option is of particular interest, if parameters like PSRR or CMRR are to analysed.

The control-source-level includes the following ideal sources:

- Voltage Controlled Voltage Source VCVS
- Voltage Controlled Current Source VCCS
- Current Controlled Voltage Source CCVS
- Current Controlled Current Source CCCS

The "transistor level" uses the MOS model, which is described in chapter 2 and the Ebers-Moll bipolar model. Up to six different parameter sets can be used during one simulation. The simulations are split into DC-analysis, small signal analysis and transient analysis.

- The DC analysis computes the DC voltages and currents in a simulated circuit. The DC-operation point -DCOP- and the DC-transient characteristic may be extracted.

- The small signal analysis -AC- is used to study the frequency domain response. Any nonlinear circuit is linearized by BONSAI before the small signal analysis is carried out.

6.1.1 Transient Analysis

The transient analysis can be computed in two different ways:

- the state variable analysis SVA
- the modified nodal analysis MNA

6.1.1.1 The State Variable Analysis (SVA)

The SVA approach needs a network that includes capacitor and inductors as memory elements. This network can be computed if two conditions are met:
1. the network is defined by voltages and currents at the start of the simulation and
2. the external stimuli are properly defined during the simulated interval. To compute the nodal states, the internal energies of the memory elements are used. The BONSAI integration procedure is the explicit or forward Euler integration. Because the SVA needs "memory" nodels, meshes consisting of voltage sources and capacitances or current sources and inductors are not allowed for a SVA method. Because the nodal matrix does not allow ideally controlled sources, in which the currents are not defined at start of simulation, that is at time t=0, the controlled sources are not allowed in the SVA approach.

6.1.1.2.a Nodal Analysis (NA)

The nodal analysis uses a matrix system based on the conductances of all nodels related to ground (0V). With the help of Kirchhoff's Voltage Law (KVL) and Current Law (KCL) all of the element conductances can be computed. This method has two advantages:

1. The equation system is always defined
2. The NA can be used for dynamic, DC, and if complex variables are used, AC analysis.

6.1.1.2.b The Modified Nodal Analysis (MNA)

Mostly based on NA, the modified nodal analysis can handle elements in its matrix system that cannot be described by conductances. This is achieved by an additional row and column in the matrix. The additional column is used for the current through the element. The current is still undefined, hence the additional row needs a "1" or a "-1" to fulfil the KCL/KVL.
Therefore, the MNA is able to analyse controlled sources.

6.1.2 Step Width Automation

BONSAI requires no defined step width. The automation procedure is based on the actual nodel value and the nodel value of the previous step. If the program detects a variation outside the error limit, a new iteration process with a reduced step width will be done. This procedure is limited by DEFAULT to 20 iterations and a voltage error of 1mV. These can be altered by the user.

6.2 Advantages over other Tools

In the field of analogue simulation, many software tools exist. The most important factors to consider when comparing such computer programs are the computer time and the stability criterion.

SPICE and BONSAI are two software packages that fulfil the industrial requirements. It has been found by Sibbert [2], that DOMOS (a predecessor of

BONSAI) scores a sufficient time advantage (factor 3 to 6), when testing the same circuits. The accuracy of most simulations is within the specified limits in both programs. It has to be noted here, that high-gain analogue building blocks show a lot of stability problems when using Spice. This is due to the integration procedures used in Spice. Appendix III show the integration procedures, that are used in BONSAI (Euler, Trapezoidal) and Spice (Gear).The Gear method is more critical in the high gain simulation than the trapezoidal method used in BONSAI.

6.3 The SC - Simulator

The SC-Simulator [3] was written because BONSAI or other comparable tools are not programmed to analyse big circuit blocks, that consist of a great many building blocks. The stimulus to create the SC-simulator was to enable the simulation of Sigma-Delta A to D converters. 19 different library elements are implemented in the SC package. Each element is described by its voltage transfer function in the time domain for the steady state. Therefore no transient characteristics can be analysed and each element needs a characterisation done by BONSAI or measurement in order to specify the analogue parameter set of the appropriate building block. Up to 50 different voltage sources can be used as stimuli to control the circuits. The manual to use this program with some more useful information is given as Appendix 4.

6.4 Simulation Results of the Analogue Building Blocks

6.4.1 Simulation Techniques

The building blocks presented in chapter three were simulated by using the BONSAI program. Before discussing the simulation results, the simulation strategy will be presented.

First of all, the DC-operating point (DCOP) must be determined. In spite of the auto-zero technique used in all of the circuits, the DC-OP should be near the midpoint voltage. The midpoint voltage is the central voltage of the power supply. Designing the DC-OP near midpoint voltage contributes to a more symmetrical characteristic during offset measurement (auto-zeroing). The DC-OP is simulated by shorting the output with the inverting input and in the case of an operational amplifier by additional stimulating the positive input with an ideal voltage of half the supply voltage. It is obvious that the resulting DC-OP point is normally outside the ideal central voltage, so the designer must make his mind about trimming the device by varying the width of one or more transistors. Before doing this, the operation area of the transistor to be trimmed (linear, saturation or near pinch off) must be checked. Assuming that the transistor operates near pinch off, the trimming process done using BONSAI or SPICE is a very critical action, because the iteration process around pinch off is not very accurate. Hence in this case it is better to accept a little inaccuracy of the simulated results. Another way to achieve higher design quality is to fix the DC-OP point or the geometry of the transistors by using measured transistor characteristics. The next parameter of common interest is the DC-transient (DC-TR) curve. The DC-TR gives all of the DC-OPs over the range of the input and output voltages. This parameter can be described as the steady state characteristic. After completion of both DC-simulations, the transient parameters must be simulated. The transient simulations are split into rise-, fall- and settling- times. Rise and fall times must be fixed between two transient points of the output voltage. In CMOS designs these points are normally the 10% and 90% values of the power supply range. The settling time is the time in which the output voltage is within the limits of relative accuracy. The relative accuracy is the accuracy of the actual voltage value over the ideal voltage value. If the building block does not achieve the specified parameters, the geometries of the transistors must be changed and the full simulation process repeated. The last simulations are the AC-characteristics. These are open loop gain, CMRR and the PSRR values. The

CMRR and PSRR parameters are achieved as the difference values of the open loop gain against the common mode gain or power supply gain. This difference can easily be done by using the TPLOT program in which the arithmetic operations are included.

6.4.2 Simulation of the Transfer-gate

Before simulating the building block, the design of the inverters must be fixed. Using an inverter as a clock booster needs a big geometry ratio and using an inverter as a transfergate component needs a geometry that fulfils the demand of accuracy and the minimizing of clock-feed-through. As there is a standard procedure to develop an inverter based on two transistors, this procedure is not explained explicitly.

As shown in chapter 3, the transfer gate operates as a unipolar switch. To minimize the parasitic influences mostly induced by the clock-feed-through charge, the geometry of the transistors is balanced. Figures 6.1 to 6.4 show the simulation results of a transfer-gate that is controlled by a symmetrical clock, which is produced by a clock generator (series connection of large geometry inverters). The input voltage is 1V. The first two figures show the characteristics with a load capacitance at the output of the transfer-gate of 5pF, the last two figures were simulated with 2pF load capacitance. The remaining clock feed-through error charge is to be seen after the falling clock edge. This error charge is bigger if the load capacitance is smaller. This characteristic is described in the equations presented in chapter 3. The currents flowing through the transfer-gate are shown in figures 6.2 and 6.4 in relation to the time window that is to be seen in the figures 6.1 and 6.3.

Figure 6.1: The falling edge of the clock change forces an error voltage at the output node.

Figure 6.2: The charges flowing through the transfergates are monitored. The error

charge is the last little current peak.

Figure 6.3: The same as figure 6.1, but the load capacitance is smaller.

Figure 6.4: The same as figure 6.2, but the load capacitance is smaller.

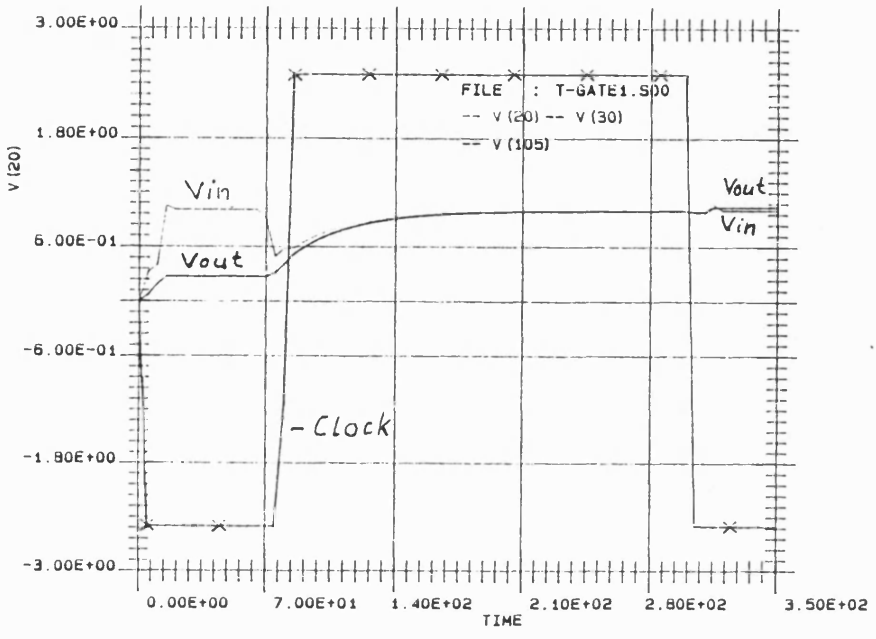

Figure 6.1 Transfer-gate with Cl=5pF voltage characteristic

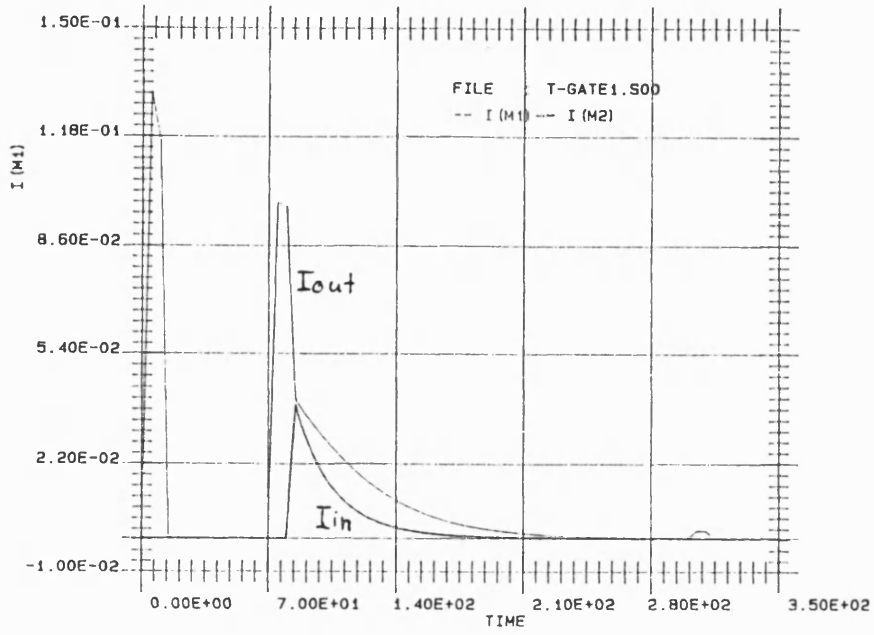

Figure 6.2 Transfer-gate with Cl=5pF current characteristic

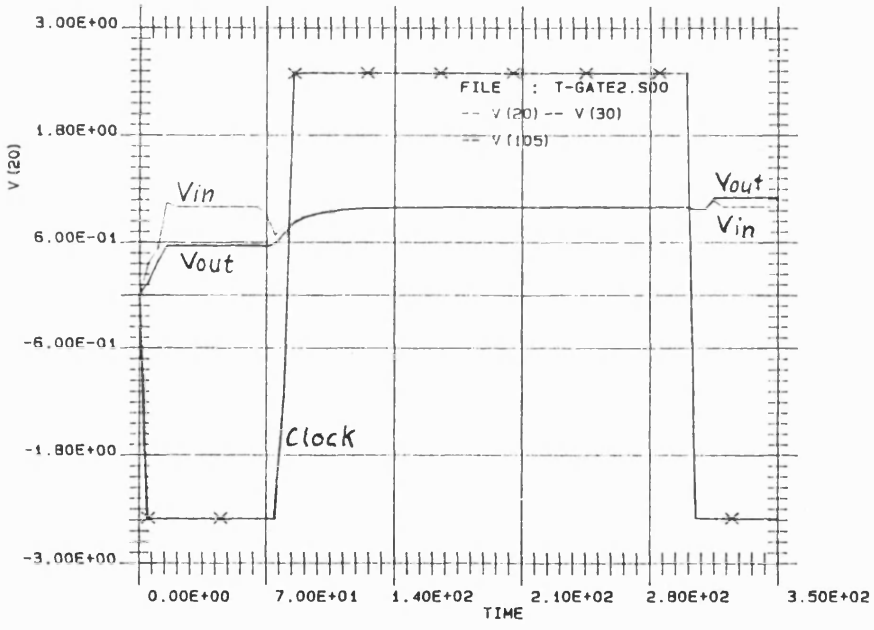

Figure 6.3 Transfer-gate with Cl=2pF voltage characteristic

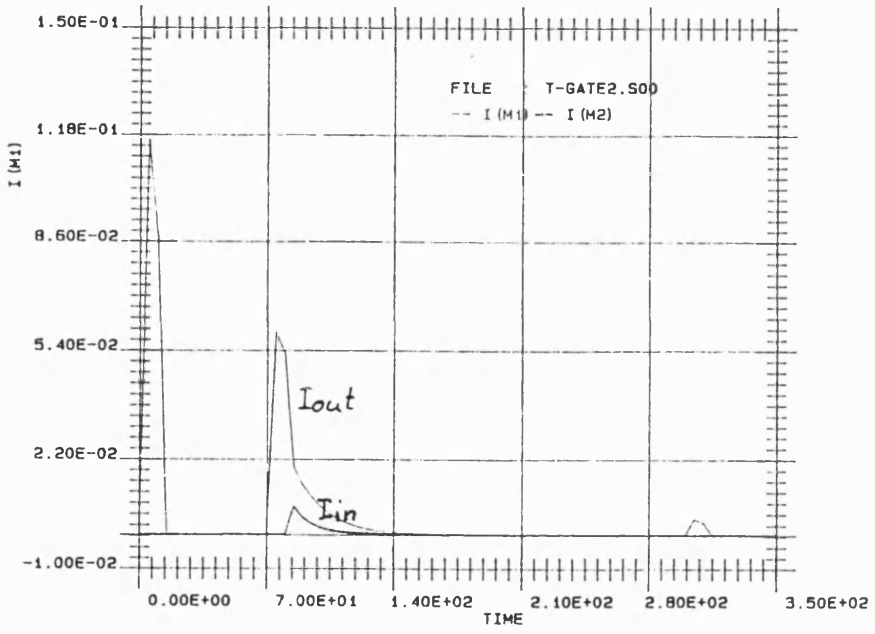

Figure 6.4 Transfer-gate with Cl=2pF current characteristic

Appendix V show the BONSAI input file and the two BONSAI output files that corresponds to the simulation results shown above, showing the accuracy as a dependence of the load capacitance.

It is to be seen that the accuracy of the output voltage does not reach the input level if the load capacitance is too big. Otherwise enlarging the transistor geometries results in an increase of the clock-feed-through sensitivity because of increasing the overlap and gate capacitance values. Hence a compromise between transitor size and load capacitance must be found. Figure 6.3 shows the same simulation results for CL=2pF. The output value was reached, but the clock-feed-through error charge was increased. In the following chapters, designs will be presented which limit the influence of the clock-feed through by using fully symmetrical concepts.

6.4.3 Simulation Results of the Cross Coupled Comparator

Based on the theoretical background presented in chapter 3.2 an ac-cross coupled comparator was developed to fulfil the high demands of accuracy and speed for use in A to D converters. Shown in [4] this building block was derived by using the ideas of standard auto-zero design techniques and a switched cross coupled auto-zero comparator. To hold the remaining offset produced by the transfer-gates as low as possible, this design also needs symmetrically designed transfer-gates. The effects of finite amplifier gain, clock-feed-through and the resistance of the transfer-gates are all limiting the quality of the switched-capacitor (SC) design. By using fully symmetrical concepts, the effect of parasitic charges are minimized. Shown in [4], the AC-cross coupled comparator is preferred for use in all the designs presented in this work. Figure 3.2.10 shows the circuit design. The following table shows the BONSAI input file.

```
.TITLE AC-CROSS COUPLED COMPARATOR
.TITLE W.TENTEN
.TITLE 10.10.1988

.INCLUDE PARM3U.BO
.INCLUDE INV_CMP
.INCLUDE INV_OUT
.INCLUDE INV_TR
.INCLUDE TG_GR_TR

.TEMP 25
.CIRCUIT
```

```
XTG_1 80 10 100 101 99 98 TG
XTG_2 85 10 110 111 99 98 TG
XTG_3 85 20 100 101 99 98 TG
XTG_4 80 20 110 111 99 98 TG
XTG_5 11 12 110 111 99 98 TG
XTG_6 21 22 110 111 99 98 TG
XINV1 11 12 99 98 INV_CMP
XINV2 21 22 99 98 INV_CMP
XINV3 12 13 99 98 INV_OUT
XINV4 22 23 99 98 INV_OUT
CI1 10 11 0.5
CI2 20 21 0.5
CC1 11 22 5
CC2 12 21 5
CL1 13  0 1
CL2 23  0 1

XINV5  100 101 99 98 INV_CL
XINV6  110 111 99 98 INV_CL
VPHI   100 0  5  0 -2.5 80 2 2 300
VPHIN  110 0 -5 10  2.5 60 2 2 300
C_CL101 101 0 2
C_CL111 111 0 2

VIN    80 0  1.256
VREF   85 0  1.255
VDD    99 0  2.5
VSS    98 0 -2.5
```

```
.CHECK
ELEMENTS ALL
.OUTPUT PRINT
V(10) V(20) V(11) V(21) V(12) V(22) V(13) V(23)
V(100) V(101) V(110) V(111)
.TRANSIENT MNA 5 0 700
.END
```

Table 6.1 BONSAI input file of the AC-Cross Coupled Comparator

Figures 6.5 to 6.8 show the BONSAI simulation plots of the following control features:

Vdd = 2.5V Vss = -2.5V

Fig.6.5: Vin-Vref = 1mV

Fig.6.6: Vin-Vref = -1mV

Fig.6.7: Vin-Vref = 1mV alternating

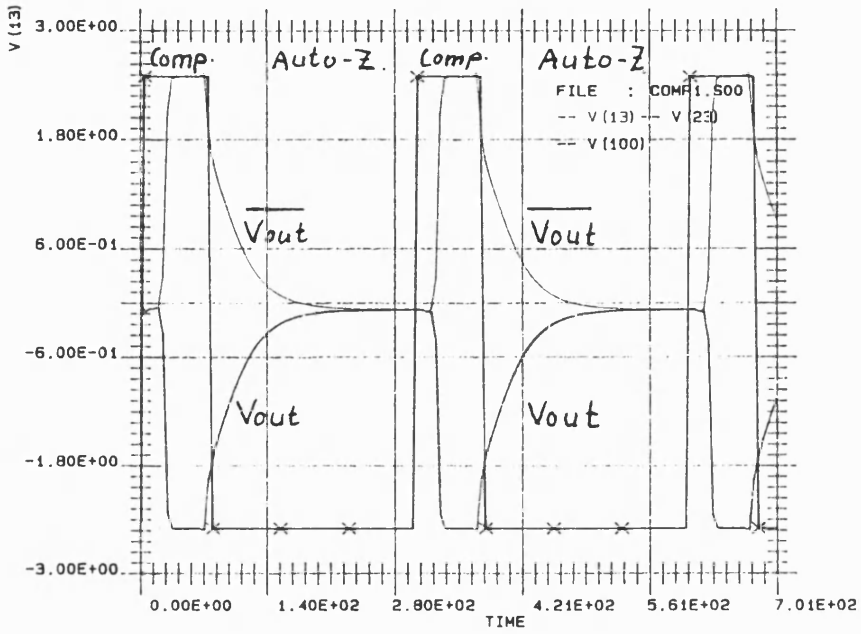

Figure 6.5 AC-Cross Coupled Comparator: 1mV

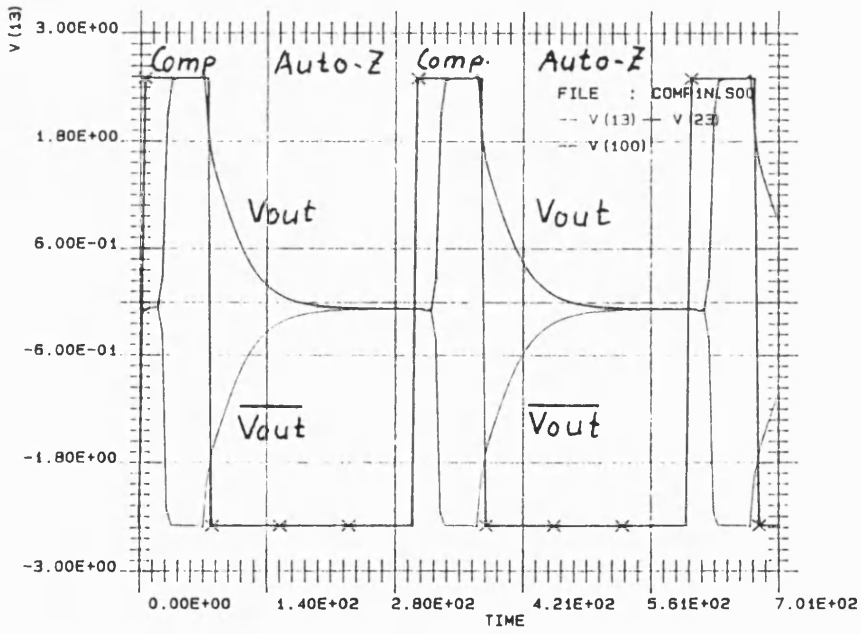

Figure 6.6 AC-Cross Coupled Comparator: -1mV

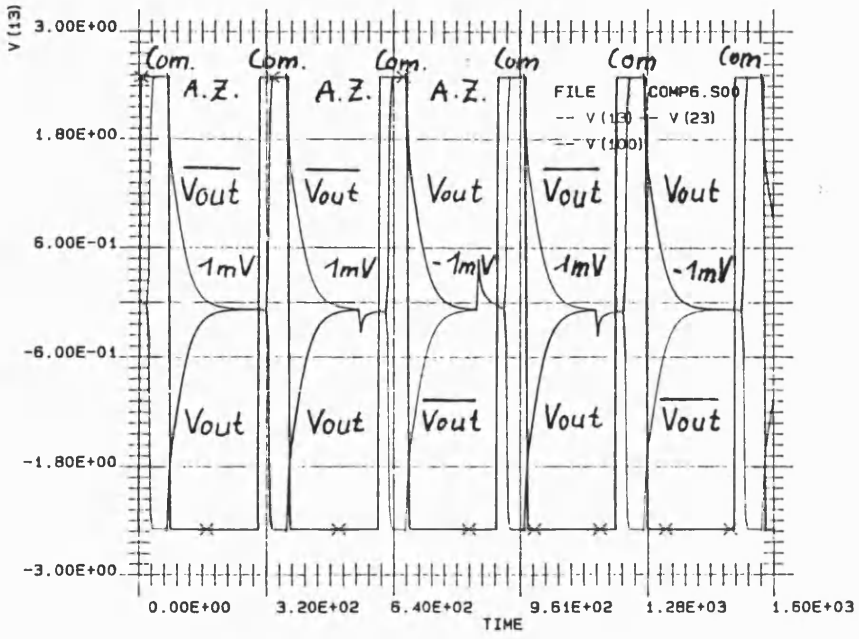

Figure 6.7 AC-Cross Coupled Comparator: alternating with 1mV

The simulations show that this type of comparator is insensitive to clock-feed-through error charge because of its fully symmetric design techniques. The resulting resolution is below 1mV. It is very difficult to simulate the final resolution, if the accuracy is below 1mV. This is dependent of the internal accuracy of the computer facility. Noise derived from numerical computation and the great number of multiplications during an iteration interval, which must be very large due to the very low error limit, is the reason for the limit of accuracy achieved by any simulation.

6.4.4 Simulation Results of the OTA Designs

6.4.4.1 Chopper OTA

Based on the theoretical description drawn in chapter 3.3, two chopper OTAs were developed and their results will now be presented:

1. Standard chopper OTA with a current controlled cascoded output [5]
2. Based on 1. Fully Symmetrical OTA with CCC-output [6]

Based on the standard OTA with auxiliary nulling input, the following simulation process was adopted for both chopper OTAs:

1. Simulation of the DCOP
2. Simulation of the DCTR
3. Simulation of the transient characteristics
4. Simulation of the ac-characteristics
5. After completion the simulation loops above:
   Simulation of the chopper circuit.

Simulations of highly sophisticated circuits like chopper OTAs built using identical amplifiers and some transfer-gates needs a lot of simulation time. Experience with simulation instruments show simulation times that can extend to hours or more than a day. Therefore using a voltage controlled voltage source (VCVS) as an auxiliary circuit for an OTA contribute to simulation times of a few 10s of minutes. Figure 6.8 shows the auxiliary chopper OTA based on a VCVS circuit.

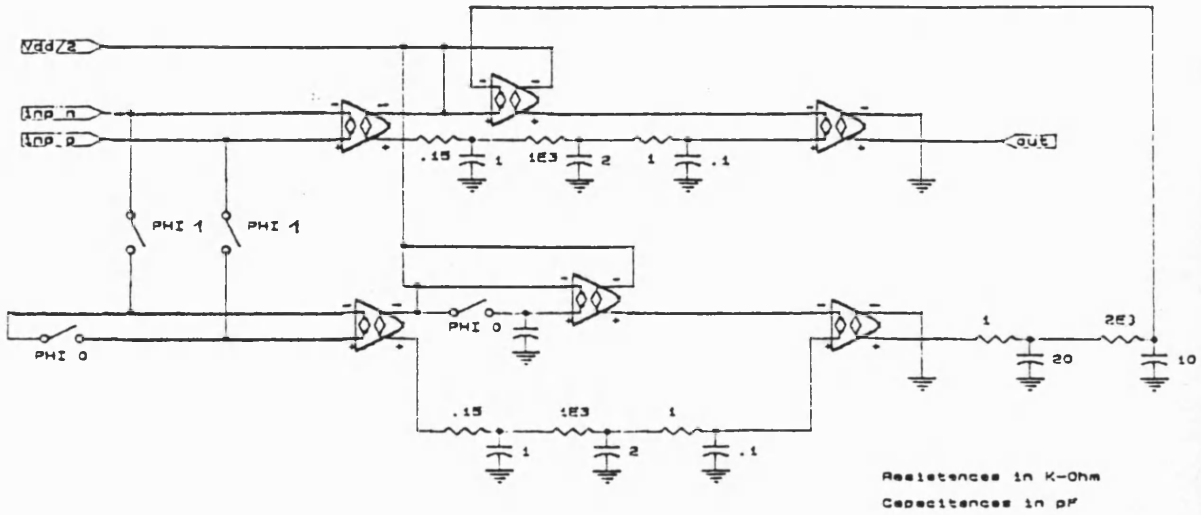

Figure 6.8 Chopper OTA based on a Voltage Controlled Voltage Source

The following table 6.2 shows the BONSAI input file of the chopper OTA simulation.

```
.TITLE SYMMETRIC OTA WITH CURRENT CONTROLLED CASCODE
.TITLE W.TENTEN  08.01.1989
.TEMPERATURE 25
$
.NOSUM
.INCLUDE PARM3U.BO
.INCLUDE INPUT.SOT
.INCLUDE CCCST.SOT
.INCLUDE OUTPUT.SOT
.INCLUDE REVERSE.SOT
.INCLUDE WIDLAR
```

```
.CIRCUIT
$    INN INZERO1 INZERO2 INP OUTP OUTN OUT BIAS KASKP KASKN VDD
VSS
XINPM  10 0    91   20 30   40     14        99 98 INP
XREV1M 40                  45          99 98 REV
XOUT1M           30 45      100    15  16  99 98 OUT
XCCC1M                      14 15  16  99 98 CCCST

XINPN  10 90   0    20 130  140    14        99 98 INP
XREV1N 140                 145         99 98 REV
XOUT1N           130 145    101    115 116  99 98 OUT
XCCC1N                     14 115 116  99 98 CCCST

XWIDL                      14         99 98 WIDLAR

RTP  101 91 2E6
CTP  91 98 10
CL1  100 98 20

VDD   99  0  2.5
VSS   98  0 -2.5
VP    20  0  0
VN    10  0  0
VZERO1 90  0 .09E-3

.LIMIT 500
.CHECK
ELEMENTS ALL
```

```
.OUTPUT PRINT
V(30) V(40) V(30) V(45) V(100) V(101)
.DCOP
.OUTPUT PRINT
VDB(100) VP(100) VDB(101) VP(101)
.AC VN 90 1 1E9
.END
```

Table 6.2 BONSAI input file of an chopper OTA ac-simulation

The following tables show the appropriate sub-building blocks:

Table 6.3: Widlar current source for I=50uA

Table 6.4: OTA input

Table 6.5: Reverse stage

Table 6.6: Current controlled cascode control circuit

Table 6.7: Output stage

```
$              BIAS VDD VSS
.SUBCIRCUIT WIDLAR 1   99  98
MP1  2  2 99 99 P  36  9  ( 36*13) ( 36*13) ( 36+ 2*13) ( 36+ 2*13)
MP2  1  2 99 99 P  36  9  ( 36*13) ( 36*13) ( 36+ 2*13) ( 36+ 2*13)
MN1  2  1  3  3 N 144  9  (144*13) (144*13) (144+ 2*13) (144+ 2*13)
MN2  1  1 98 98 N  16  9  ( 16*13) ( 16*13) ( 16+ 2*13) ( 16+ 2*13)
R1 3 98 16
```

Table 6.3 Widlar current source

```
$          IN- INZERO1 INZERO2 IN+ OUTP OUTN BIAS VDD VSS
.SUBCIRCUIT INP 20  25    26    30  5   4   40   99  98
$
$NR  D  G  S  B T  W   L  AD   AS   PD   PS
$
MP1  4  4 99 99 P 109  3  (109*13) (109*13) (109+ 2*13) (109+ 2*13)
MP2  5  5 99 99 P 109  3  (109*13) (109*13) (109+ 2*13) (109+ 2*13)
MN1  4 20  7  7 N 250  3  (250*13) (250*13) (250+ 2*13) (250+ 2*13)
MN2  5 30  7  7 N 250  3  (250*13) (250*13) (250+ 2*13) (250+ 2*13)
MN3  7 40 98 98 N  80  9  ( 80*13) ( 80*13) ( 80+ 2*13) ( 80+ 2*13)
$
$ ADDITIONAL INPUT STAGE FOR THE NULLING SECTION
$
MN10  4 25 17 17 N 125  3  (125*13) (125*13) (125+ 2*13) (125+ 2*13)
MN11  5 26 17 17 N 125  3  (125*13) (125*13) (125+ 2*13) (125+ 2*13)
MN12 17 40 98 98 N  40  9  ( 40*13) ( 40*13) ( 40+ 2*13) ( 40+ 2*13)
```

Table 6.4 OTA input

```
$          IN OUT VDD VSS
.SUBCIRCUIT REV 1  2   99  98
$
$NR  D  G  S  B T  W   L  AD   AS   PD   PS
$
MP4  2  1 99 99 P 500  3  (500*13) (500*13) (500+ 2*13) (500+ 2*13)
MN5  2  2 98 98 N 140  3  (140*13) (140*13) (140+ 2*13) (140+ 2*13)
```

Table 6.5 Reverse stage

```
$              BIAS KASKP KASKN VDD VSS
.SUBCIRCUIT CCCST    40  4    2    99  98
MP1  2  1 99 99 P 119  3  (119*13) (119*13) (119+ 2*13) (119+ 2*13)
MP2  1  1 99 99 P 119  3  (119*13) (119*13) (119+ 2*13) (119+ 2*13)
MP3  4  4  1 99 P 119  3  (119*13) (119*13) (119+ 2*13) (119+ 2*13)
MN1  2  2  3 98 N  80  3  ( 80*13) ( 80*13) ( 80+ 2*13) ( 80+ 2*13)
MN2  3  3 98 98 N  80  3  ( 80*13) ( 80*13) ( 80+ 2*13) ( 80+ 2*13)
MN3  4 40 98 98 N  48  9  ( 48*13) ( 48*13) ( 48+ 2*13) ( 48+ 2*13)
```

Table 6.6 Current controlled cascode control circuit

```
$          INP INN OUT KASKP KASKN VDD VSS
.SUBCIRCUIT OUT 4   5   10  50   60   99  98
$
$NR  D  G  S  B T  W   L  AD   AS   PD   PS
$
MP4  8  4 99 99 P 561  3  (561*13) (561*13) (561+ 2*13) (561+ 2*13)
MP5 10 50  8 99 P 561  3  (561*13) (561*13) (561+ 2*13) (561+ 2*13)
MN6 10 60  9 98 N 140  3  (140*13) (140*13) (140+ 2*13) (140+ 2*13)
MN5  9  5 98 98 N 140  3  (140*13) (140*13) (140+ 2*13) (140+ 2*13)
```

Table 6.7 Ota output

The simulation results of the chopper OTA is shown in the following table 6.8 [5].

Parameter unit	OTA	Chopper OTA (C-OTA)
Supply voltage (V)	5	5
Common mode range (V)	V_{Th} to Vss-V_{Th}	V_{Th} to Vss-V_{Th}
Slew rate (V/usec)	10	20
t settle 1% (usec)	0.9	0.8
Load capacitance (pF)	20	20
Unity gain freq. (MHz)	20	20
Phase margin (degrees)	40	40
CMRR (dB)	73	125
PSRR-Vdd (dB)	39	40
PSRR-Vss (dB)	38	40
A_{DC} (dB)	60	110
$f_{chopper}$ (PHI1,2) (Hz)		500

$f_{SC\text{-}R}$ (PHI3) (Hz)		4000
V_{Off} (mV)	10	<0.05

Table 6.8 Simulated results of the OTA and the chopper OTA

The following figures show the plots of the simulated OTA and chopper OTA.

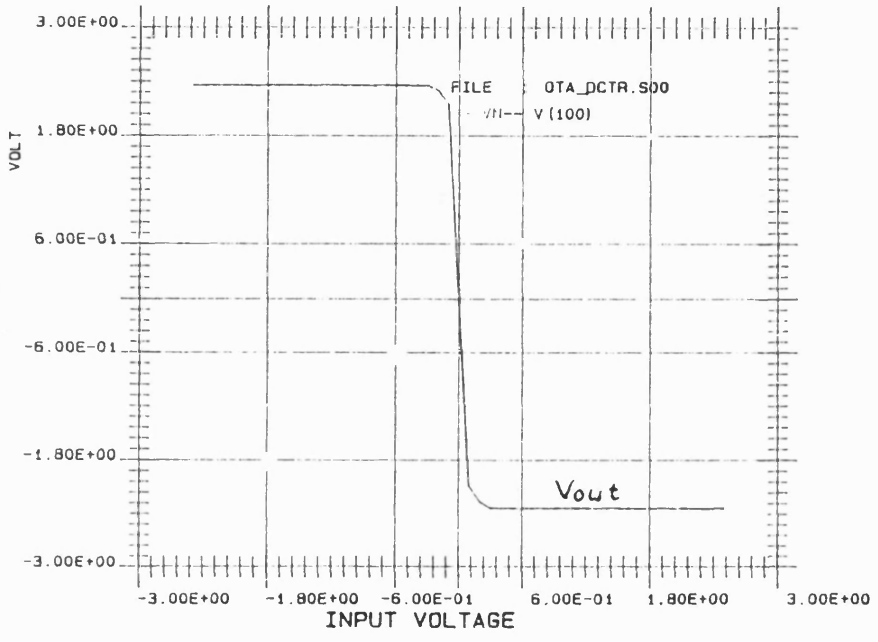

Figure 6.9 OTA DC-transient characteristic

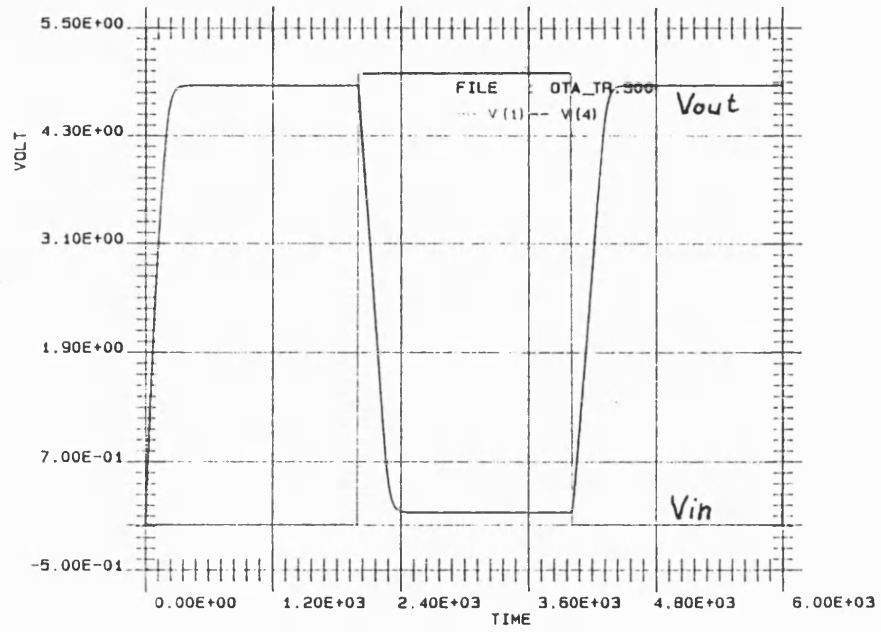

Figure 6.10 OTA transient characteristic

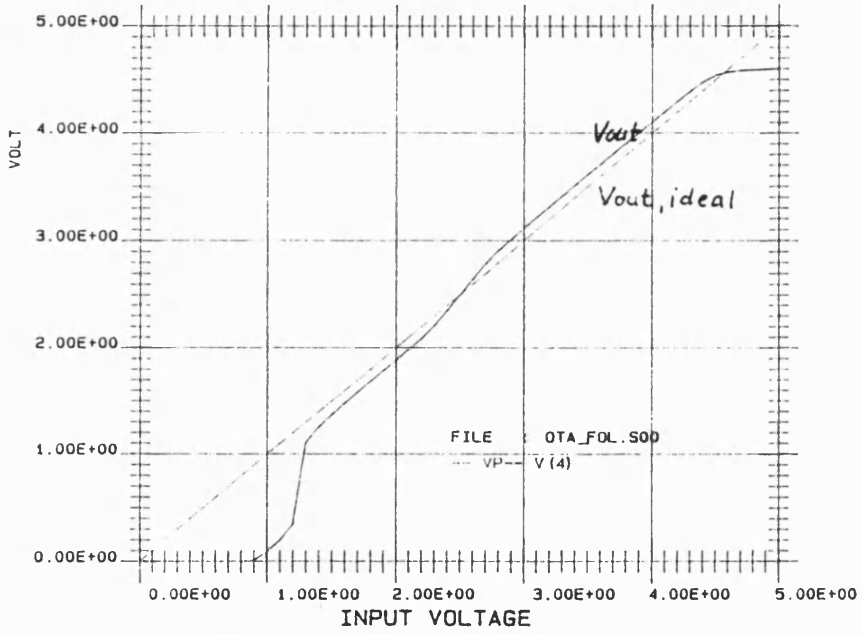

Figure 6.11 OTA voltage follower characteristic

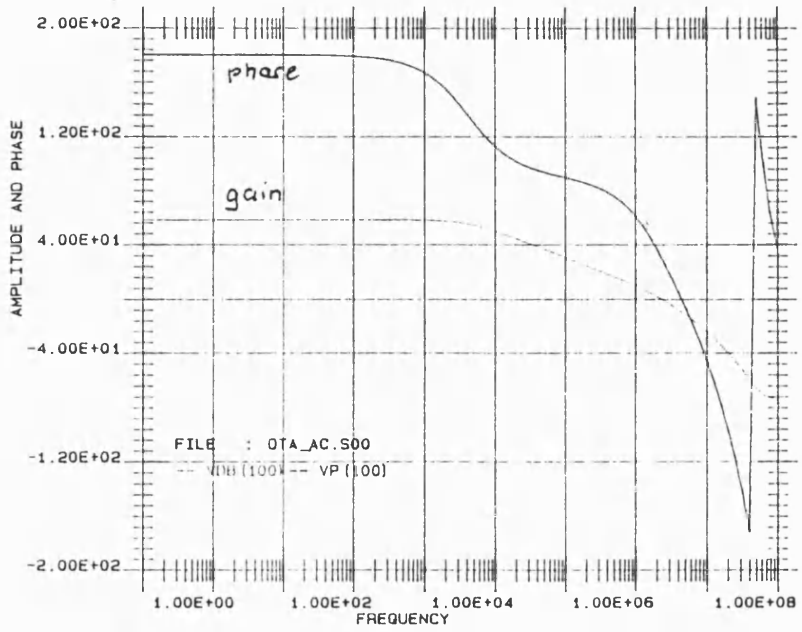

Figure 6.12 OTA ac-characteristic

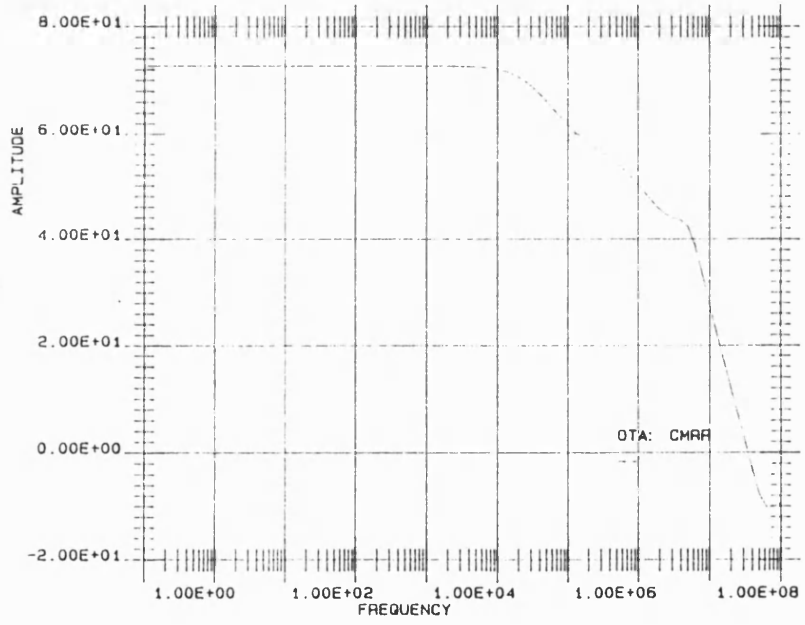

Figure 6.13 OTA CMRR characteristic

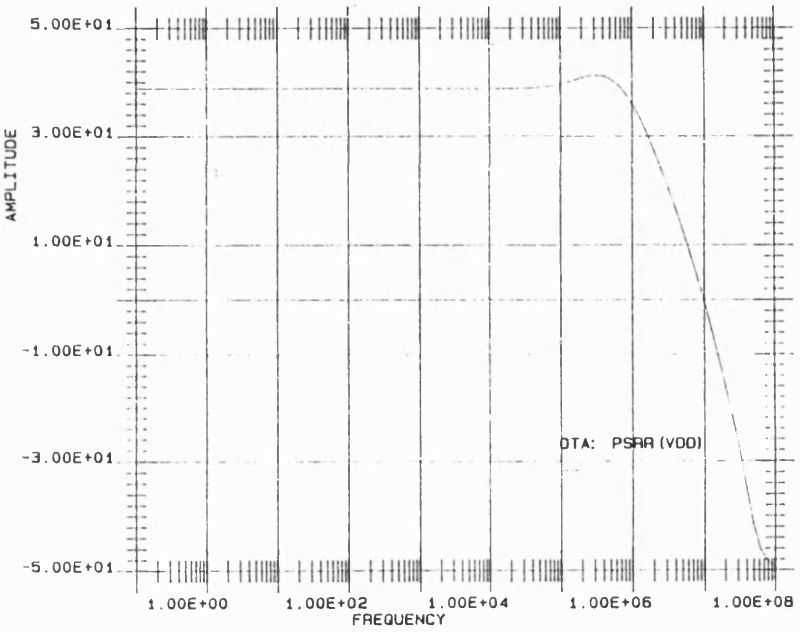

Figure 6.14 OTA PSRR(Vdd) characteristic

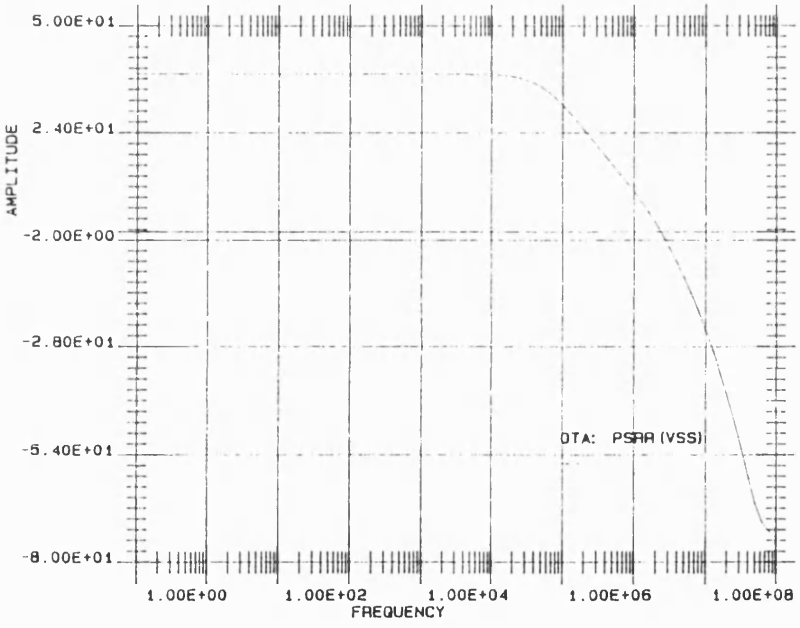

Figure 6.15 OTA PSRR(Vss) characteristic

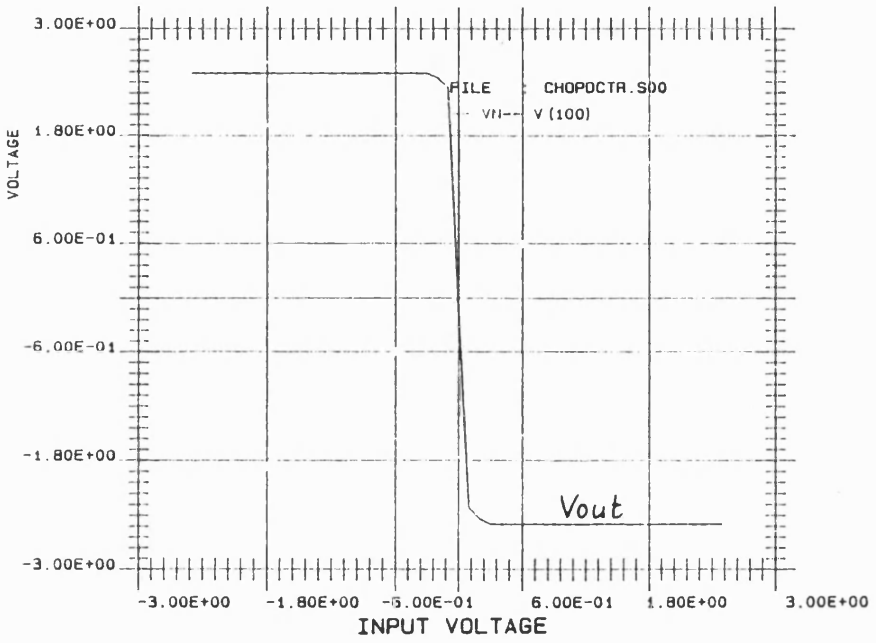

Figure 6.16 C-OTA DC-transient characteristic

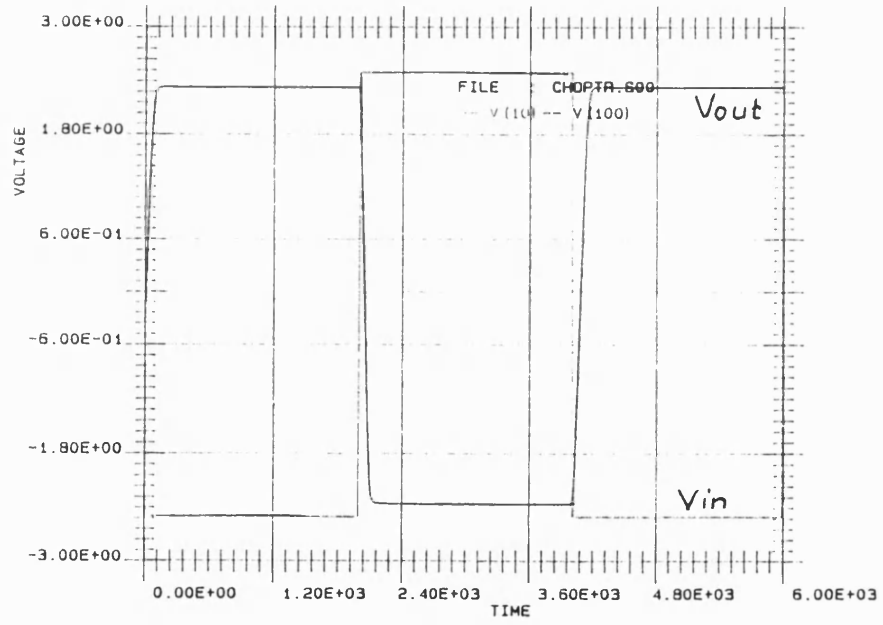

Figure 6.17 C-OTA transient characteristic

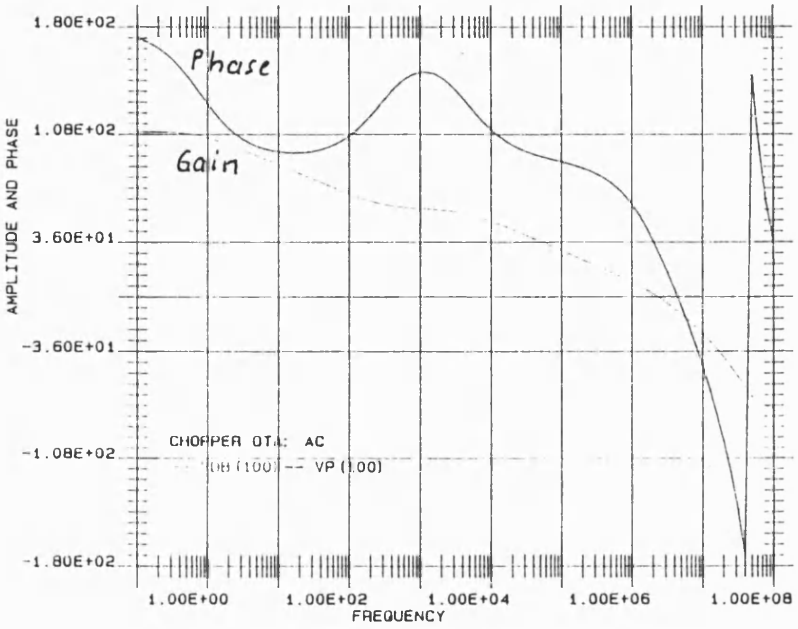

Figure 6.18 C-OTA ac-characteristic

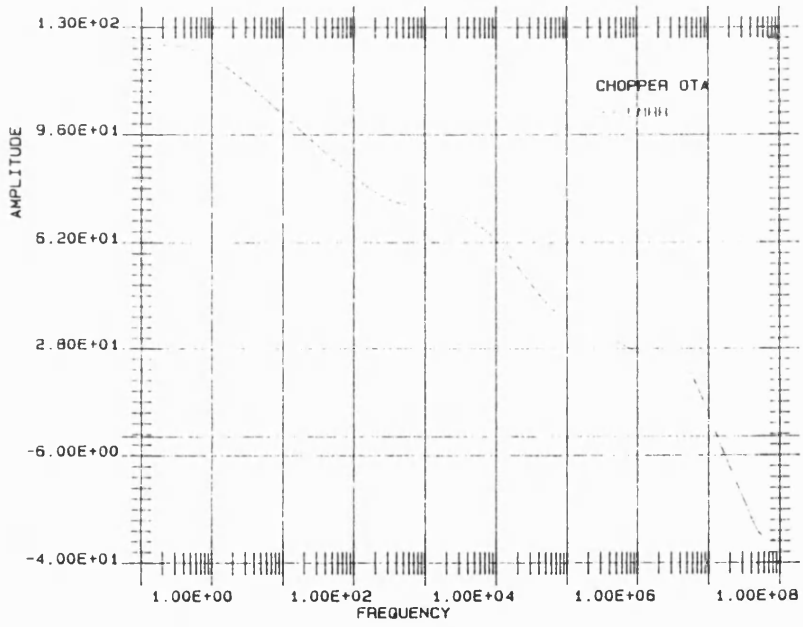

Figure 6.19 C-OTA CMRR characteristic

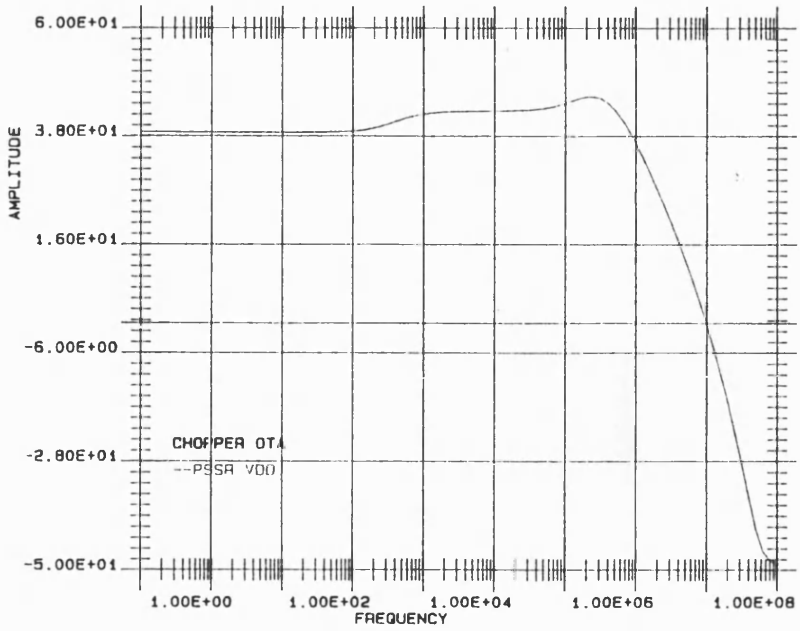

Figure 6.20 C-OTA PSRR(Vdd) characteristic

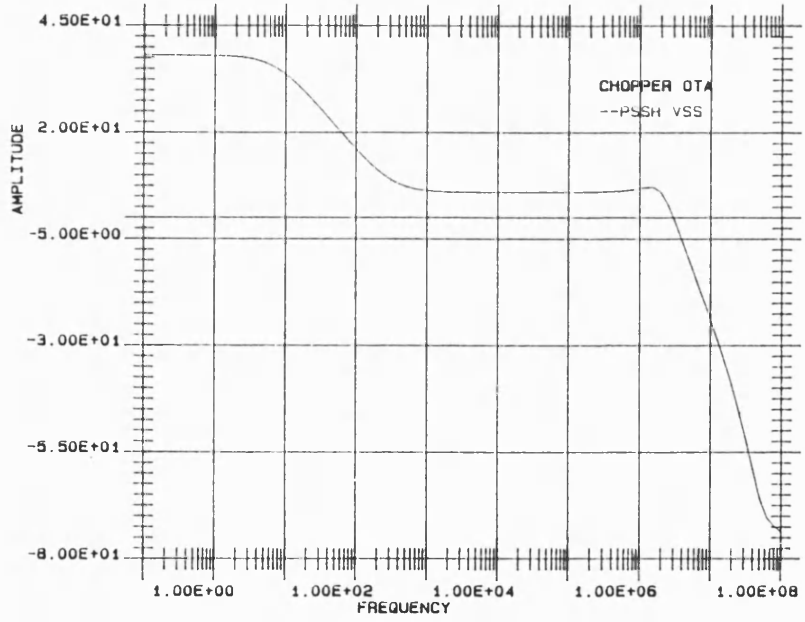

Figure 6.21 C-OTA PSRR(Vss) characteristic

The simulation results shown above fulfil the demands for the use in high quality analogue to digital converter designs. In particular the characteristics of the chopper OTA contributes to higher performace in low frequency designs. Sensor applications using base bands up to about 10kHz for example would benefit from the use of these circuits. Higher accuracy can be achieved by using fully symmetrical design techniques. In particular the influence of the clock-feed-through can be minimized and the power supply rejection is increased in the lower frequency range. Table 6.9 shows the simulated results of the fully symmetric OTA (SOTA) and the fully symmetric chopper OTA (SC-OTA) [6].

Parameter (Unit)	SOTA	SC-OTA
Supply voltage (V)	5	5
Common mode range (V)	V_{Th} to Vss-V_{Th}	V_{Th} to Vss-V_{Th}
t settle 1% (usec)	0.9	0.8
Slew rate (V/usec)	25	25
Load capacitance (pF)	20	20
Unity gain freq. (MHz)	15	15
Phase margin (degrees)	20	20
CMRR (dB)	73	133

PSRR-Vdd (dB)	39	96
PSRR-Vss (dB)	38	96
A_{DC} (dB)	60	115
$f_{chopper}$ (PHI1,2) (Hz)		500
f_{SC-R} (PHI3) (Hz)		4000
V_{Off} (mV)	10	<0.05

Table 6.9 Simulated results of the fully symmetric OTA and choppered OTA

The following tables 6.10 and 6.11 shows the BONSAI input file of a typical simulation of the SOTA and the SC-OTA.

```
.TITLE SYMMETRIC OTA WITH CURRENT CONTROLLED CASCODE
.TITLE  W.TENTEN  08.01.1989
.TEMPERATURE 25
$
$
.INCLUDE PARM3U.BO
.INCLUDE INPUT.SOT
.INCLUDE CCCST.SOT
.INCLUDE OUTPUT.SOT
.INCLUDE REVERSE.SOT
.INCLUDE WIDLAR
```

```
.CIRCUIT
$    INN INZERO1 INZERO2 INP OUTP OUTN OUT BIAS KASKP KASKN VDD
VSS
XINP  10 90    91    20 30  40      14          99 98 INP
XREV1              30         35              99 98 REV
XREV2              40         45              99 98 REV
XOUT1                30  45  100    15   16   99 98 OUT
XOUT2                40  35  110    17   18   99 98 OUT
XCCC1                          14  15   16   99 98 CCCST
XCCC2                          14  17   18   99 98 CCCST
XWIDL                          14          99 98 WIDLAR

CL1  100 98  20
CL2  110 98  20

VDD   99  0  2.5
VSS   98  0 -2.5
VP    20  0  0
VN    10  0 -2.5
VZERO1 90  0 -3.415E-1
VZERO2 91  0 -3.415E-1

.CHECK
ELEMENTS ALL
.OUTPUT PRINT
V(10) V(20) V(100) V(110)
V(30) V(35) V(40) V(45) V(14) V(15) V(16) V(17) V(18)
.DCOP
```

```
.CIRCUIT
VN   10 0 5 0.5E3 -2.5 .5E3 1 1 2E3
.OUTPUT PRINT
V(10) V(20) V(100) V(110)
V(30) V(35) V(40) V(45) V(14) V(15) V(16) V(17) V(18)
.TRANS MNA 1 0 2E3
.END
```

Table 6.10 BONSAI input file of the fully symmetrical OTA

```
.TITLE SYMMETRIC CHOPPERED OTA WITH CURRENT CONTROLLED
CASCODE
.TITLE W.TENTEN  08.01.1989
.TEMPERATURE 25
$
$
.INCLUDE PARM3U.BO
.INCLUDE INPUT.SOT
.INCLUDE CCCST.SOT
.INCLUDE OUTPUT.SOT
.INCLUDE REVERSE.SOT
.INCLUDE WIDLAR

$            INN INP NULLN NULLP OUTP OUTN VDD VSS
.SUBCIRCUIT SYM-OTA 10  20  90   91   100  110  99  98

$   INN INZERO1 INZERO2 INP OUTP OUTN OUT BIAS KASKP KASKN VDD
VSS
```

```
XINP  10 90   91   20 30  40     14        99 98 INP
XREV1           30       35          99 98 REV
XREV2           40       45          99 98 REV
XOUT1             30  45  100   15   16   99 98 OUT
XOUT2             40  35  110   17   18   99 98 OUT
XCCC1                    14  15   16   99 98 CCCST
XCCC2                    14  17   18   99 98 CCCST
XWIDL                    14        99 98 WIDLAR

.CIRCUIT
XOTAM 1 2 11 12  8  7 99 98 SYM-OTA
XOTAN 1 2 90 91 18 17 99 98 SYM-OTA
RTP1  17 11 2E6
RTP2  18 12 2E6
CTP1  11 98 10
CTP2  12 98 10
CLM1   8 98 20
CLM2   7 98 20

VDD   99  0  2.5
VSS   98  0 -2.5
VP     2  0 -1 * VN
VN     1  0  5 .5E3 -2.5 .5E3 1 1 2E3
VZERO1 90  0 -3.415E-1
VZERO2 91  0 -3.415E-1

.CHECK
ELEMENTS ALL
```

```
.OUTPUT PRINT
V(1) V(2) V(7) V(8) V(17) V(18) V(11) V(12)
.TRANS MNA 1 0 2E3
.END
```

Table 6.11 BONSAI input file of the fully symmetrical chopper OTA

Both fully symmetric OTA designs are based on the basic sub-building blocks of the OTA shown in tables 6.3 to 6.7. Therefore the simulation techniques can directly be derived by those of the standard OTA simulation runs. The following figures show the plots of the simulated SOTA and choppered SC-OTA.

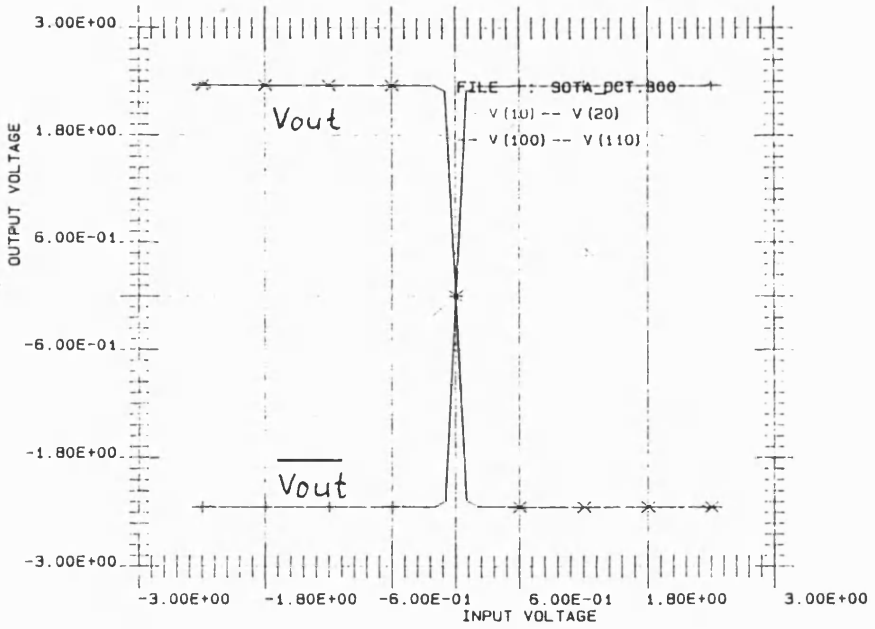

Figure 6.22 SOTA DC-transient characteristic

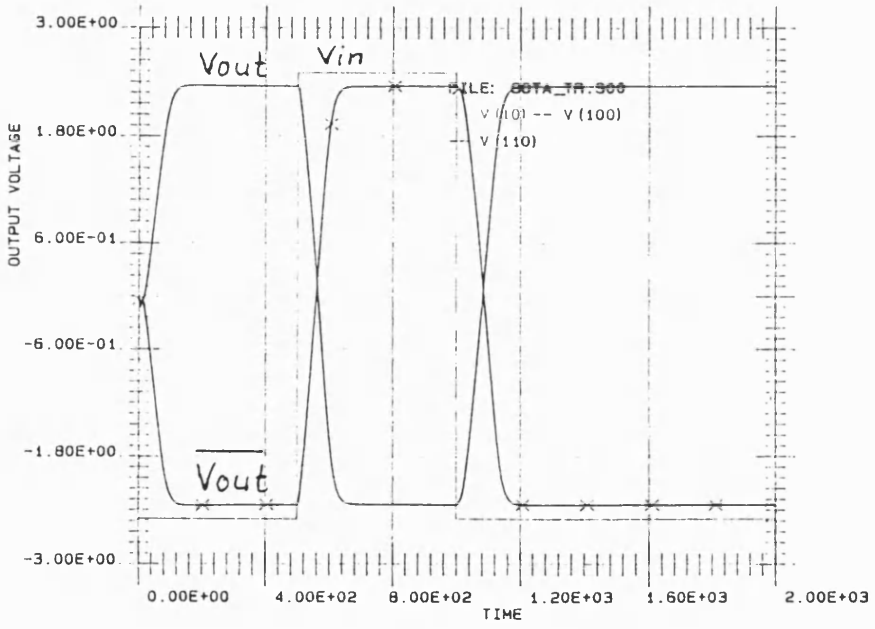

Figure 6.23 SOTA transient characteristic

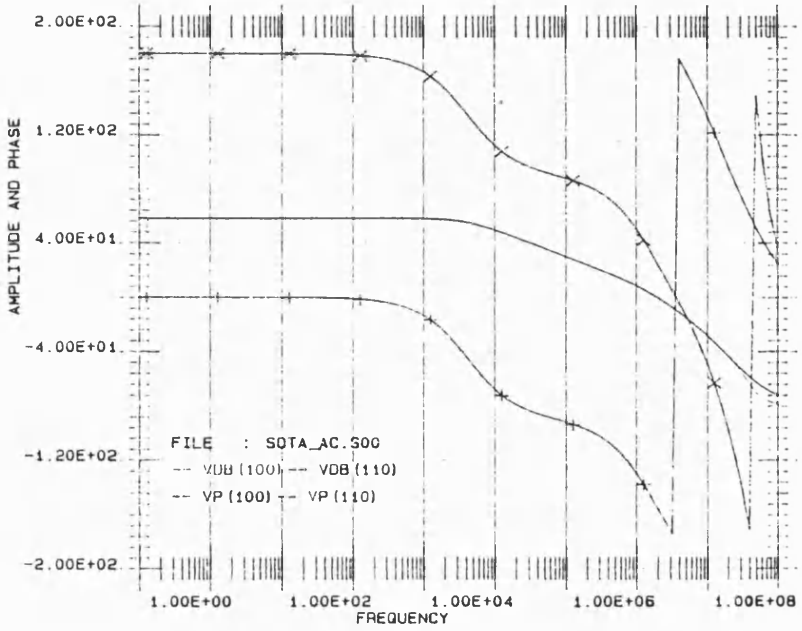

Figure 6.24 SOTA ac-characteristic

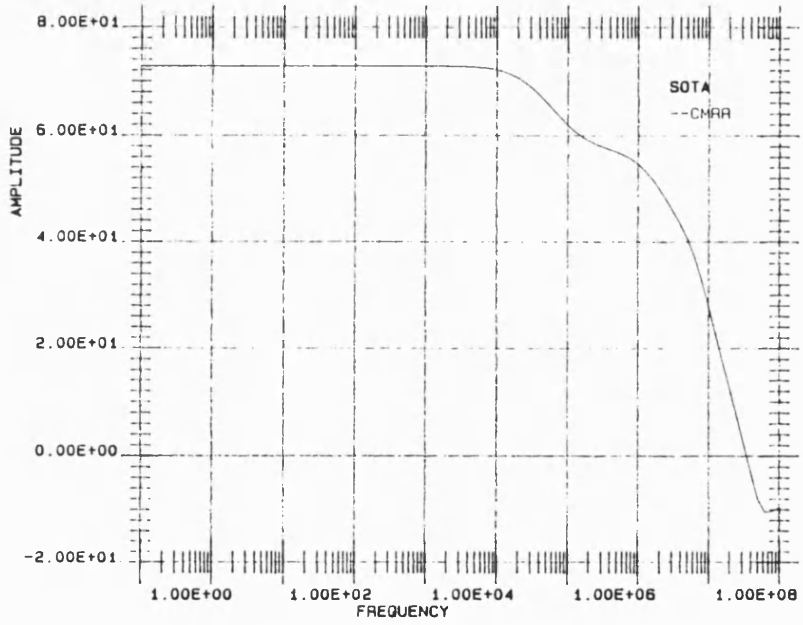

Figure 6.25 SOTA CMRR characteristic

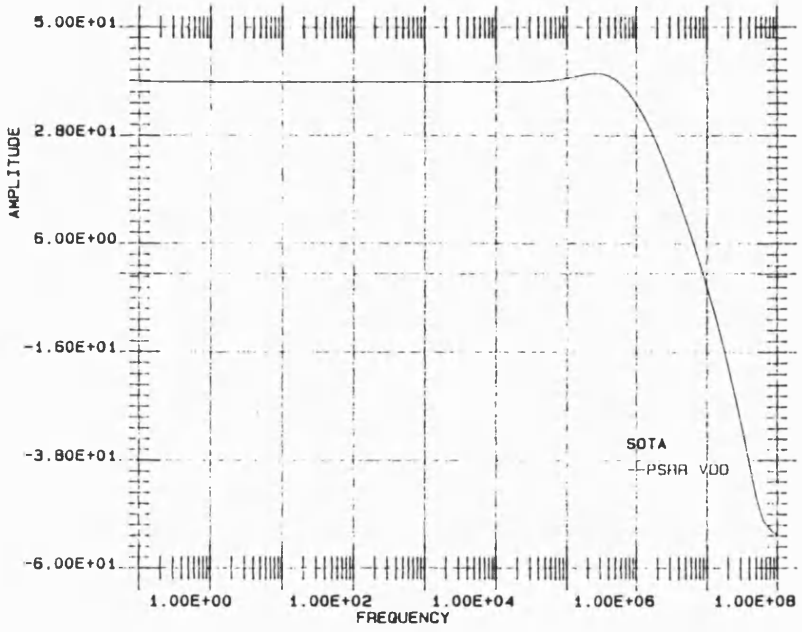

Figure 6.26 SOTA PSRR(Vdd) characteristic

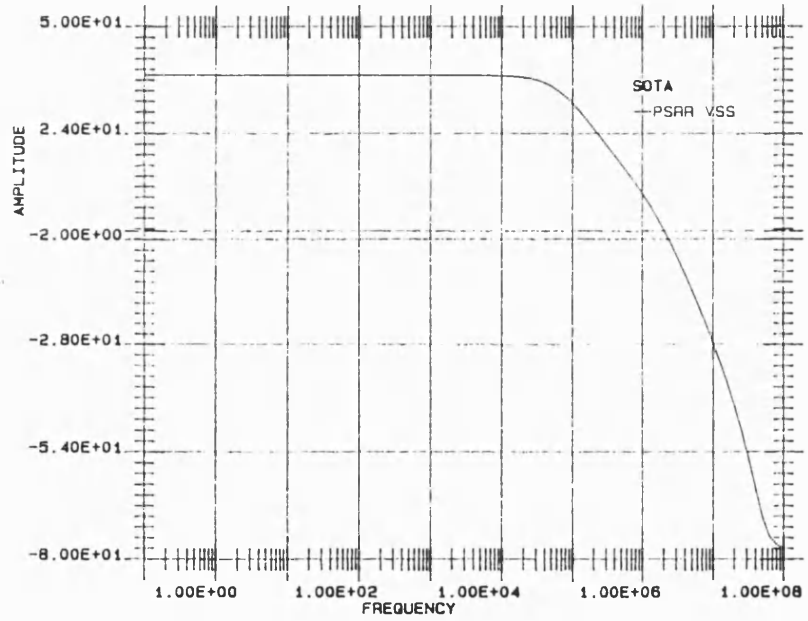

Figure 6.27 SOTA PSRR(Vss) characteristic

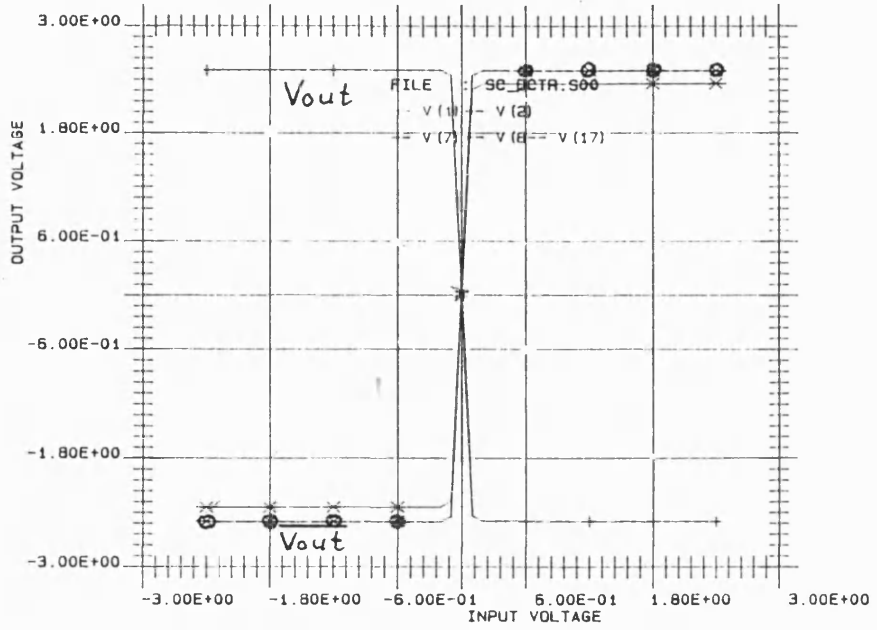

Figure 6.28 SC-OTA DC-transient characteristic

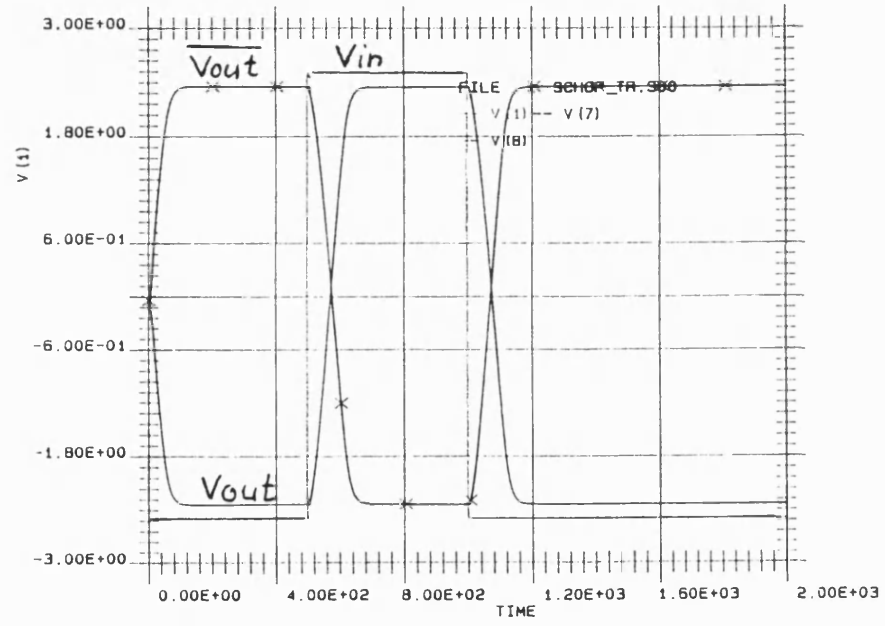

Figure 6.29 SC-OTA transient characteristic

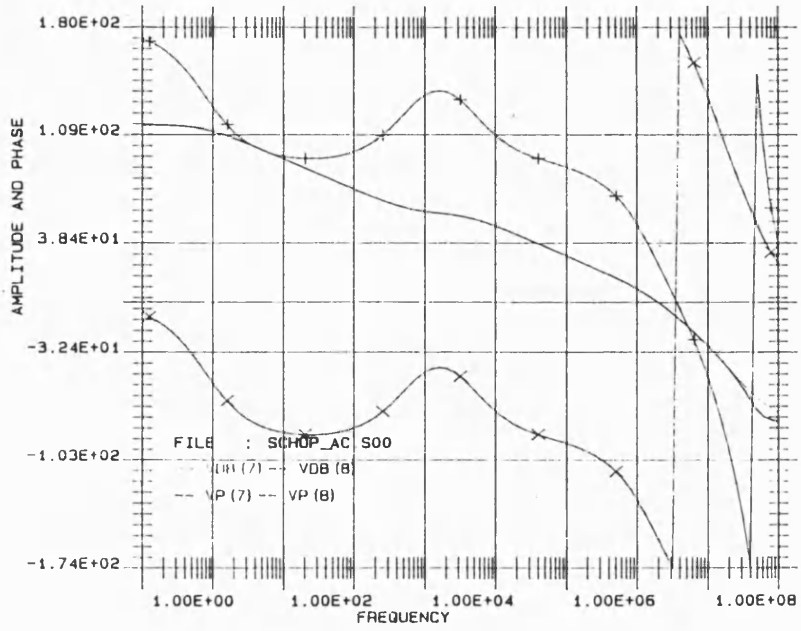

Figure 6.30 SC-OTA ac-characteristic

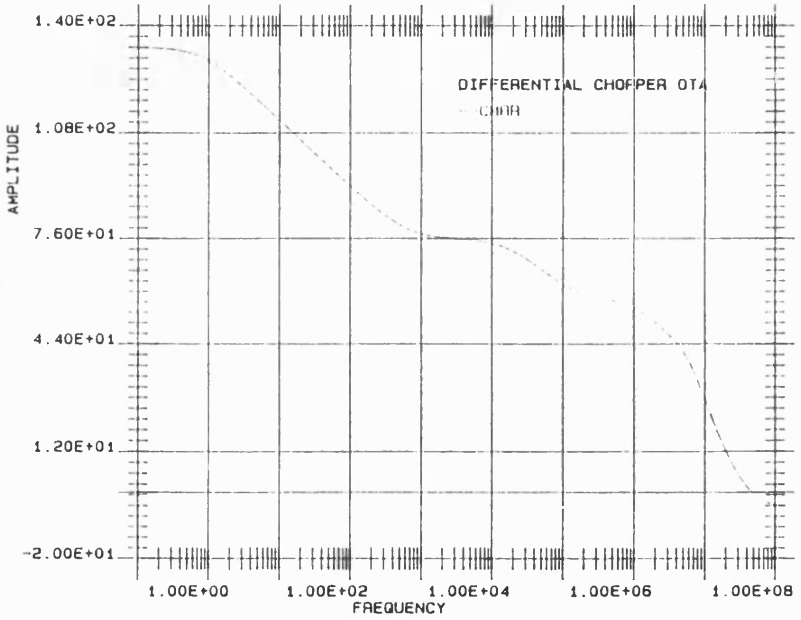

Figure 6.31 SC-OTA CMRR characteristic

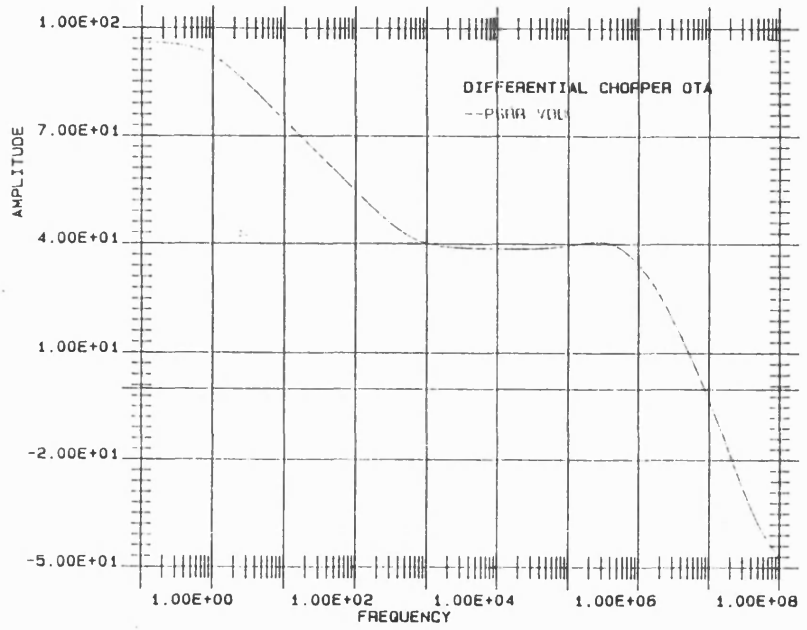

Figure 6.32 SC-OTA PSRR(Vdd) characteristic

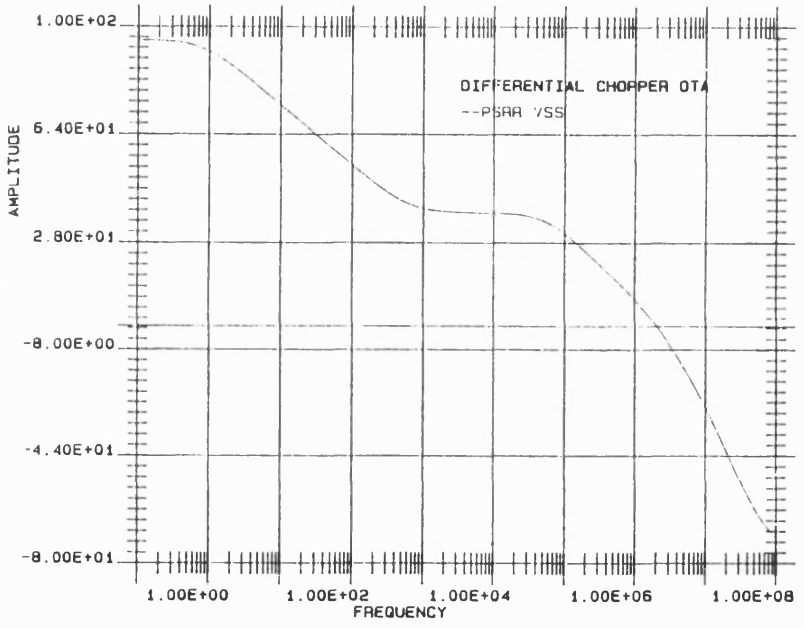

Figure 6.33 SC-OTA PSRR(Vss) characteristic

The simulations shown above characterise the building blocks used in the A to D converters, which are presented in the next chapter.

REFERENCES CHAPTER 6

[1] "BONSAI - BOsch Network and Analysis Instrument", Bosch GmbH, Microelectronic Center D-7487 Reutlingen Tübingerstr. 123

[2] Sibbert H, private communication

[3] "SC - A program to compute switched-capacitor building blocks", Tenten W. D-7487 Gammertingen, Bubenhofenstr. 7, 01.04.1989

[4] "A New CMOS High-Speed, High Accuracy Auto-Zero Comparator Design Based On Symmetric Cross Coupled Concepts", Tenten W.J., Shepherd P.R., Int.Journal of Electronics, not yet published

[5] Tenten W.J., Shepherd P.R., "Novel chopper OTA with dynamic bias control and current controlled cascoded output", Int.J,Electronics, Vol.65, No.1, pp.19-25, 1988

[6] Tenten W.J., Shepherd P.R., "Novel fully differential chopper OTA with dynamic bias control and current controlled cascoded output", to be published in Int.J,Electronics

CHAPTER 7

7. Development of Improved ADC Circuits

Analog to Digital Converters (ADC) have been presented in a great many variety of CMOS technologies over the last decade. Preferred for industrial applications are the McCreary switched capacitor array ADC (e.g. Siemens ADC 0810) and, increasingly, the sigma delta ADC (SD-ADC) principle (e.g. ITT ADC2300E Audio A/D Converter). The resolution of the Siemens device is 8 bit by 10 bit accuracy and the ITT SD-ADC has a 13 bit resolution with 1/2 LSB accuracy.

Using the components and the VIS reference circuits presented in chapters 3 and 5, six ADCs will be presented. The principles used are the Suàrez two-capacitor array (see chapter 4), the algorithmic principle, the incremental principle and the delta-sigma principle.

7.1 The VIS Controlled Suàrez Analogue to Digital Converter

This principle was selected to show the improvement quality obtained by choosing the VIS technique to perform the charge splitting during the successive approximation steps. Figure 7.1 shows the circuit drawing of the ADC. A V-VIS or an I-VIS can be used as the reference control unit. The analogue building blocks "DELAY, MEMORY and SUMMATION" use the amplifier presented in chapter 3.3.3.2. The MEMORY block stores the analogue information, if the EXOR gate outputs a logical HIGH. The SUMMATION input is controlled by the DELAY output and the MEMORY output. The input capacitance of this ADC is feed by the SUMMATION output during phase 2.

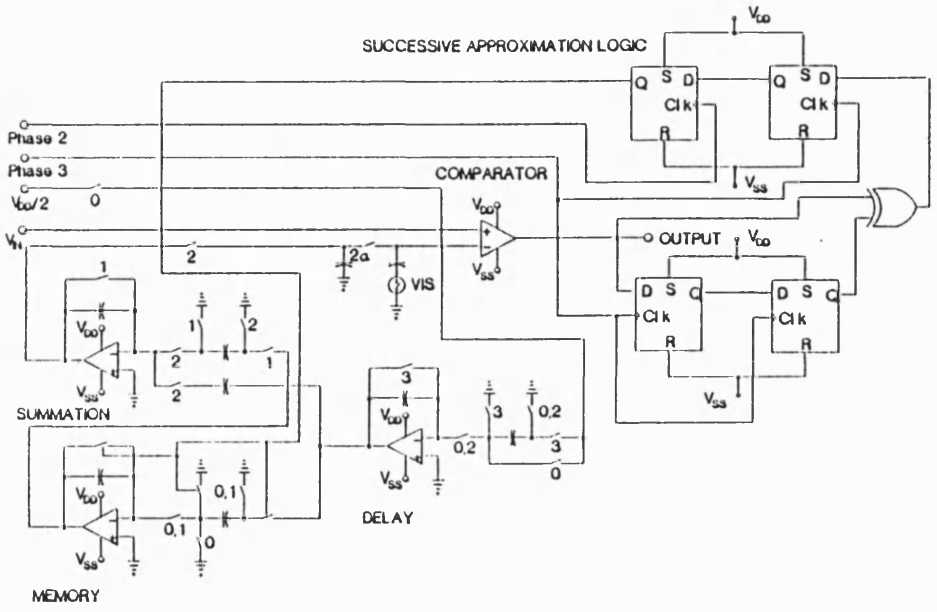

Figure 7.1 Successive Approximation VIS Controlled ADC

The circuit operation is as follows:

Step 1:

Phase-0 This is the initialisation phase. The analogue delay register is precharged with V_{dd}. The VIS output is initialized to V_{dd}

Step 2:

Phase-1 During phase 1, the summation amplifier is discharged. The VIS circuit measures its error voltage.

Step 3:

Phase-2 This phase is split into two. During the main phase, the voltage value of the VIS as a result of the step before is loaded into the analogue delay block.

The digital information from the EXOR gate, delayed by phase 3, activates the switches of the analogue memory block. A logic One controls the storage of the analogue voltage value from the step before. This value was delayed by the DELAY block. During the second part, phase 2a, the charge splitting is activated under the control of the VIS. These two sub-phases are nonoverlapping.

Step 4:

Phase-3 The VIS process is finished, the comparator outputs a logical One if the VIS output is less than the input voltage, otherwise the result of the comparison is a logical Zero. The logical number is stored in the D-Flip-Flop block and is shifted to the input of the EXOR gate during the next clock phase three. Hence the logical comparison at the input of the EXOR gate is processed by the actual digital value and the digital value of the step before. Because of this arrangement no successive approximation register is needed.

Table 7.1 shows a numerical example of the succesive approximation process.

Vin=3V

VIS-out	Delay	Memory	Comparator	EXOR
5	5	0	0	0
2.5	2.5	2.5	1	1
3.75	3.75	2.5	0	0

3.125	3.125	2.5	0	0
2.8125	2.8125	3.125	1	1
2.96875	2.96875	3.125	1	0
3.046875	3.046875	2.96875	1	1
3.0078125	3.0078125	2.96875	1	0

Table 7.1 Suàrez ADC numerical example

By using the V/I-VIS circuits and the chopper OTA building block, the accuracy is improved from 8 bit to 12-14 bit. Linearity and monotonicity are dependent on the quality of the analogue memory cells. Matching of capacitances is to below 0.1% by using a double poly processes. This error can be thought of as an overall system offset and can be cancelled by using a calibration run after every 1000 AD-cycle. This calibration run results in a digital offset word that can be added to or subtracted from the digital word of each following AD-cycle. Hence the limit factors of the quality of this ADC are the clock feed through and the quality of the VIS circuit. The chopper OTA concept needs just one nulling amplifier for all of the OTAs used within this concept. The conversion time is dependent on the specified accuracy. Table 7.2 shows the conversion time and the bandwidth as a function of the resolution and accuracy.

resolution	accuracy	1 bit conversion time	bandwidth
10 bit	2.4 mV	1.16 usec	86.2 KHz
12 bit	610 uV	1.35 usec	61.7 KHz
14 bit	153 uV	1.57 usec	45.5 KHz

Table 7.2 Accuracy against conversion time

7.2 Algorithmic Analogue to Digital Converter

Following the designs described in [1,2,3], and simplifying the idea of the algorithmic principle to its basic structure, results in an ADC shown in figure 7.2. High quality in resolution and accuracy and an inherently monotonic operation combined with a minimized number of components are the main advantages of this ADC.

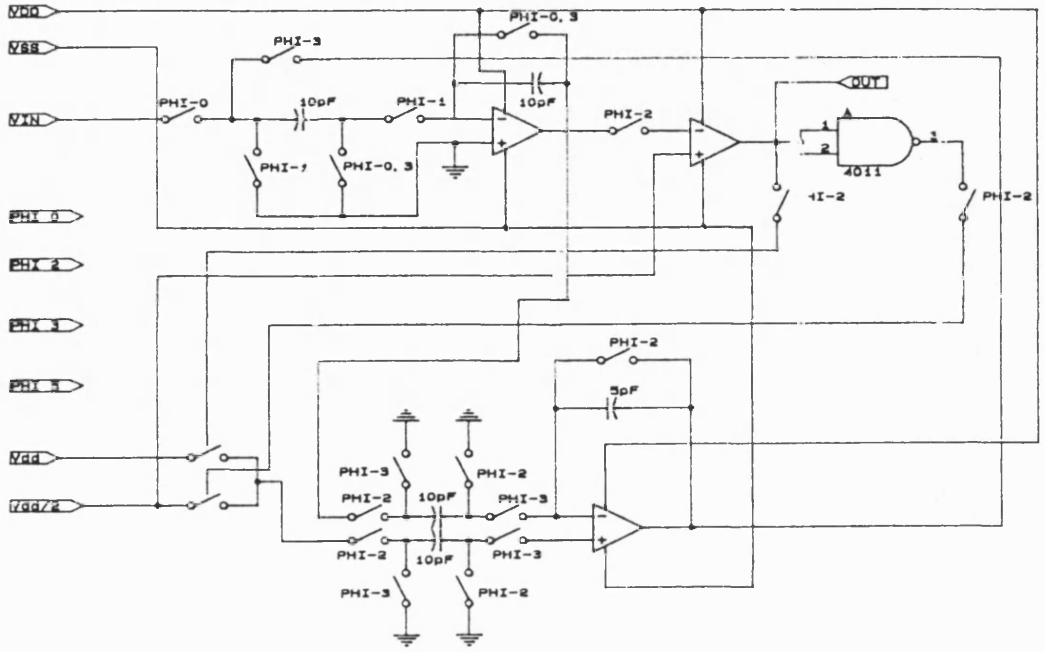

Figure 7.2 Algorithmic A/D Converter

The circuit operation is as follows:

Step 1:

Phase 0 The sample and hold (s&h) capacitor is fed by the input voltage Vin and the s&h amplifier is discharged.

Step_2:

Phase 1 The s&h capacitor is connected to the inverting input of the s&h amplifier. This circuit technique offers a stray insensitive operation, because all the nodes are connected to low-impedance sources.

Step_3:

Phase 2 The voltage stored in the s&h amplifier is output to the comparator and is stored on the input capacitance of the multiplier amplifier. Depending on the comparator's decision (logical 1, if Vs&h > Vdd/2, else logical 0), either Vdd or Vdd/2 (signal ground) feeds the other (positive input) capacitance. The multiplier is discharged.

Step_4:

Phase 3 The difference between the voltages of the input capacitances of the multiplier is divided by two. This result feeds the s&h capacitor.

All the switches are referenced to signal ground, that is identical to Vdd/2. The following table 7.3 shows the circuit operation for Vin=3V as a numerical example.

s&h amplifier	Comparator	Multiplier
3	1	(3 - 2.5) * 2 = 1
1	0	(1 - 0) * 2 = 2
2	0	(2 - 0) * 2 = 4
4	1	(4 - 2.5) * 2 = 3

Table 7.3 Numerical example of the algorithmic ADC

The accuracy of this AD-converter is directly dependent on the performance of the amplifiers and the accuracy of the factor of 2 multiplier. The inaccuracy of a capacitance array is dependent on the oxide thickness variation and on the distance between the capacitances [4].

$$\frac{\Delta C1/C2}{C1/C2} \approx \frac{\delta t_{ox}/\delta x}{t_{\overline{ox}}} \cdot L \qquad (7.1)$$

where:

tox is the oxide thicknes

$t_{\overline{ox}}$ is the averaged oxide thickness

x is one dimensional coordinate

L is the distance between the midpoints of the two capacitors

Generally best matching can be achieved by an octogonal layout technique and a proper double polysilicon process. The clock feed through can be minimized using the differential technique, whenever possible. The circuit of figure 7.2 has a simulated

efficiency of more than 12 bit without offset calibration cycles and by using offset calibration cycles in between the normal operation, the accuracy can be shifted towards the 16 bit range.

7.3 Difference Delta Sigma ADC

Based on the standard delta sigma ADC (DS-ADC) techniques proposed by Candy [5] and Temes [6], a DS-ADC was developed to introduce a difference-quantization technique. Figure 7.3 shows the principle circuit drawing of this ADC.

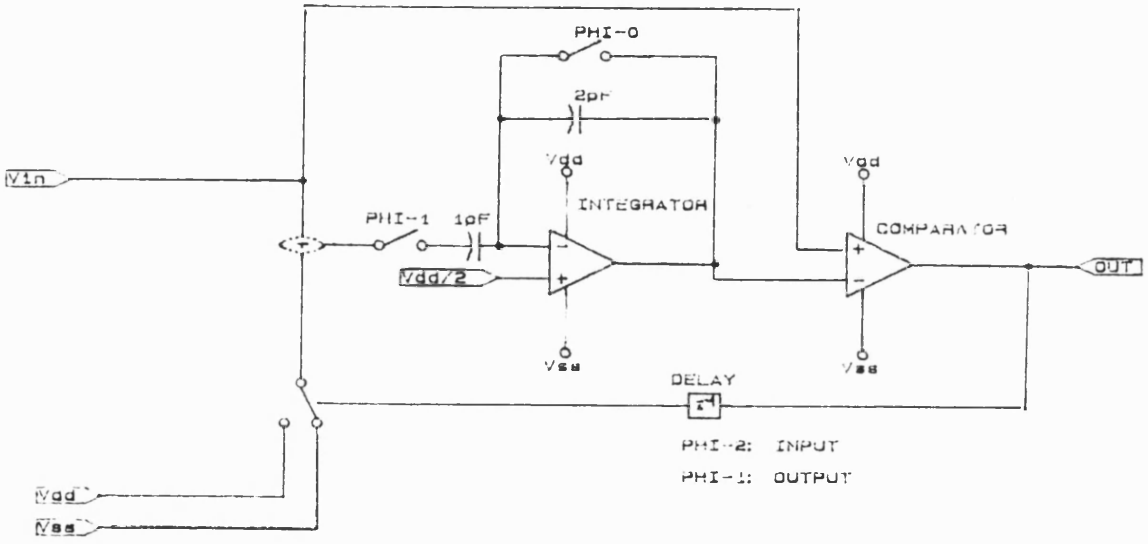

Figure 7.3 Difference Delta-Sigma Analogue to Digital Converter

The signal transfer-function of this DS-ADC is given by:

$$S = Sz^{-1} + Vin - Kz^{-1} \quad if \quad Y = High \tag{7.2a}$$

$$S = Sz^{-1} + Vin + Kz^{-1} \quad if \quad Y = Low \tag{7.2b}$$

where:

S is the output of the integrator

K is the correction voltage

Y is the output of the comparator

Vin is the actual input voltage

It is to be noted that the term z^{-1} in Sz^{-1} is used only if an inherent delayed integrator concept is used. This means that the input capacitance is fed during phase n and the integration process is done in phase n+1.

The circuit operation is as follows:

Step_1:

Phase 0 The integrator is discharged

Step_2:

Phase 1 The input voltage added with the reference (unknown at the first step) feeds the integrator.

Step_3:

Phase 2 The comparison results in a logical 1 if the integrator output voltage is greater than or equal to the input voltage. This logical data is put in a shift register and additionally in a delay register.

Step_4:

Phase 1 The delay register is read out, hence the logical as a result from the A to D phase before (z^{-1}) forces the appropriate reference voltage to be mixed with the input voltage.

The digital filter, used for this circuit technique comprises two parts, a decimation filter and a low pass filter. The decimation technique can be described thus all the digits of one oversample period are put into a full adder circuit. The decimation procedure can now be continued by building the mean value of the digits over this time-window. Because of the special difference arrangement, the appropriate digital response is always the difference between the integrator, that is the balanced response, and the actual input voltage.

The digital low pass filter needs to have a characteristic dependent on the pass band and the noise shaping effect. The baseband noise induced by the digitizing of the comparator can be described [5] for a standard Candy coder as:

$$N_0^2 = 4 \cdot e_0^2 \cdot \frac{1}{f_s} \cdot \int_0^{f_0} \sin^2 \cdot \left(\pi \cdot \frac{f}{f_s} \right) df \tag{7.3}$$

$$N_0^2 = 2 \cdot \frac{f_0}{f_s} \cdot e_0^2 \cdot \left(1 - si\left(2 \cdot \pi \cdot \frac{f_0}{f_s} \right) \right) \tag{7.4}$$

where:

τ is the period time of the sample frequency.

e_0^2 is the power spectral density of white noise. This is used here as a description of the quantization noise; if the signal is strong or active enough to produce many quantizations, then this noise can be described as a random signal.

f is any frequency within the baseband

f_0 is the upper corner frequency of the baseband

Candy uses the baseband noise built by a uniform amplitude distribution in the range +/- 0.5 (1 is full scale) and by simplifying eqn. (7.4) for the oversampled condition to:

$$N_0 = \frac{2 \cdot \pi}{\sqrt{3}} \cdot e_0 \cdot \left(\frac{f_S}{2 \cdot f0} \right)^{-3/2} \tag{7.5}$$

$$e_0 = \frac{1}{\sqrt{6}} \tag{7.6}$$

$$N_0 = \sqrt{2} \cdot \frac{\pi}{3} \cdot \left(\frac{f_S}{2 \cdot f0} \right)^{-3/2} \tag{7.7}$$

where f_s is the sample frequency.

Computing for the conditions:

fs = 2 MHz

f_0 = 10KHz

results in

N_0 = 56.56 dB

This result indicates an accuracy better than 9 bit, hence an ADC with 8 bit resolution and 9 bit accuracy can be designed. Improvements of the accuracy can be achieved by a double integration or by the MASH technique [8].

7.4 Incremental VIS contolled SD-ADC

Derived from the algorithmic principles [1,2,3,7] another self-controlled algorithm can be used: the VIS reference. Combined with the DS-ADC principle this results in a new ADC principle, called the Incremental VIS Delta Sigma ADC (IV-DS-ADC). Figure 7.4 shows the circuit drawing of this ADC.

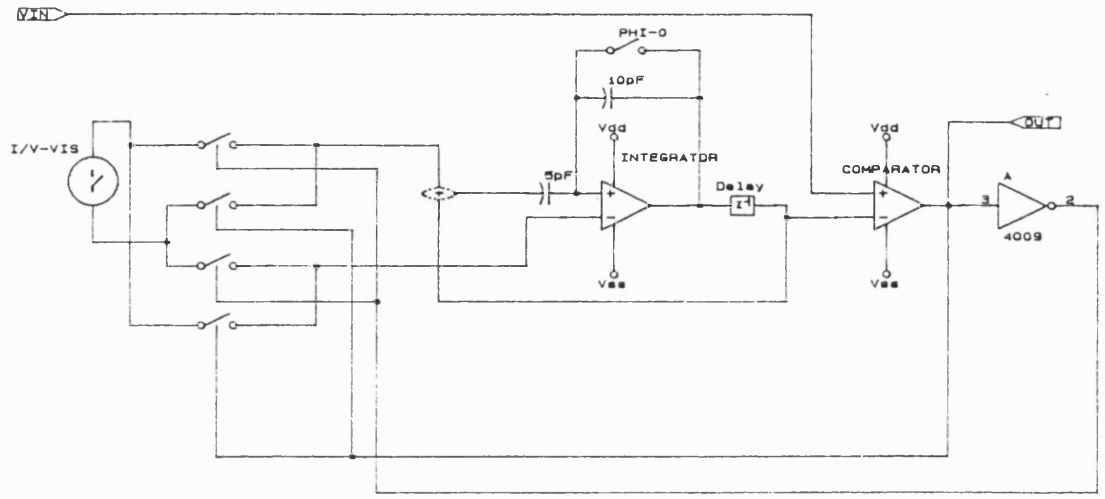

Figure 7.4 Incremental-VIS-Delta-Sigma-A/D-Converter

This circuit technique uses the VIS reference voltage steps as its internal corrections. The reference voltage is fixed for each step during the A to D cycle. Hence in comparison to the Candy-type DS-DAC, this DS-ADC has more in common with the algorithmic ADCs. The delta part and the sigma are built by the input of the amplifier as in the conventional capacitor array. The input section is different to the Candy-type DS-ADC. Here the signal is not input to the sigma part. The input is the VIS reference or signal ground, depending on the sign of the comparator. If the comparator output is high, the applied VIS reference voltage is switched to the

negative input of the integrator and signal ground is applied to the sigma input. The resulting integrated value is delayed and afterwards compared with the input voltage. Therefore this principle results in an incremental approach to the final voltage. This principle needs a sample and hold stage to hold the input signal stable over one internal ADC step. One internal ADC step includes all the steps used to achieve the desired accuracy. The resulting quantization error of the s&h input stage is frequency dependent. The internal VIS loop control gives the overall accuracy to detect the s&h step size. Assuming this VIS loop results in a 16 bit accuracy, the s&h must be sampled by a factor much bigger than 2*16 to achieve desirable results for the maximum frequency range. An overall oversampling factor of 256 is preferrable. In the case of 16 bit accuracy, the upper corner frequency of the passband is 7.812kHz, using the chopper OTA. The signal to noise ratio (S/N) of a sinusoidal signal can be derived thus:

$$V_{eff\,sine} = \frac{V}{\sqrt{2}} \tag{7.8}$$

Shown in chapter 4, the probability density function of the sine wave gives:

$$SQR \approx \frac{2}{3} \cdot 2^{2n} \tag{7.9}$$

$$SQR \approx 6.02ndB + 1.8dB$$

where:

n is the bit range.

SQR means Signal to Quantisation Ratio

The expected SQR values for a sine-wave input are shown in table 7.4.

Bit range	SQR
10	62.00dB
12	74.04dB
14	86.08dB
16	98.12dB

Table 7.4 SQR values for different bit-ranges.

It is to be noted, that the noise shaping is not established within this type of SD-ADC. The integration process that results in the noise shaping characteristic is used in standard SD-ADC's to improve the SNR by lower internal resolution. The advantage of this circuit technique is that the idea of signal summation with its history and the difference used to balance the integrator is shifted to the VIS-control loop. The monotonicity and the linearity are below 0.5 LSB, because of the internal control loop accuracy. Additionally care must be taken to avoid confusion with the signal to quantisation noise ratio SQR and the signal to noise ratio SNR. The differences were explained in chapter 4.5.2

7.5 Fully Differential Analogue to Digital Converter

The fully differential chopper OTA concept presented in chapter three offers the means of optimum error cancellation. A design that offers maximum error cancellation of the parasitic effects needs a fully symmetric signal path. Thus the input signal must be mirrored. This introdues an additional error source, which includes errors from internal limitation of gain, clock feed through etc. Hence using the idea above to handle the reference instead of the signal gives the full advantage of the building blocks shown in chapter three.

7.5.1 Incremental D-VIS Controlled A/D-Converter

Based on the circuit in figure 7.4, the fully differential OTA is used to realise the input amplifier. The VIS used for this new ADC is the D-VIS. Figure 7.5 shows the circuit drawing.

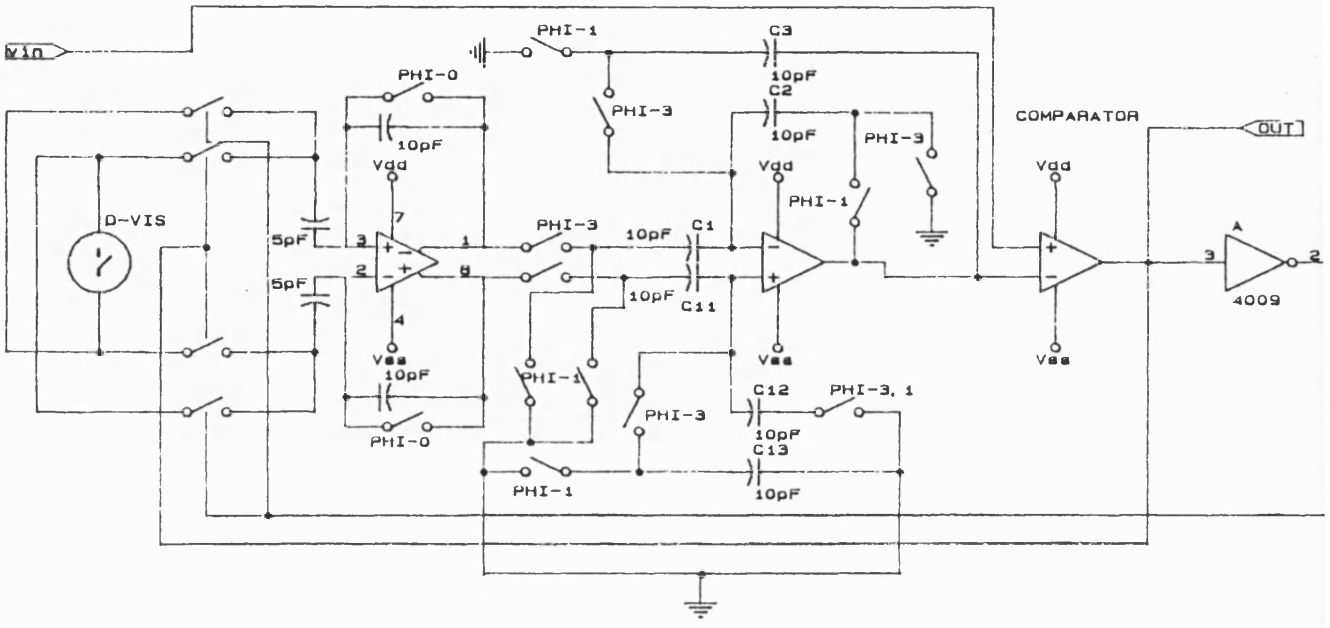

Figure 7.5 Fully Differential D-VIS Controlled Incremental ADC

The circuit operation is as follows:

Step 1:

The D-VIS is loaded with the supply voltages V_{dd} and V_{ss}, respectively. The fully differential choppered OTA (DAM) is discharged. The following amplifier is a differential to single ended opamp [2] with the advantage that the offset need be compensated. An improvement in the accuracy is achieved with the transfer-function of this device showing a A^{-2} dependence on the DC-gain. This differential to single ended amplifier (SAM) is reset during this phase.

Step_2:

The VIS circuit controls the internal precision divide-by-two operation. The result is loaded into the differential input stage.

Step_3:

The voltage of the DAM is now shifted into the SAM and is prepared for comparison. The direction of the switches between the D-VIS and the DAM is dependent on the decision of the comparator. This is an automatic incremental step without using a digital control block. The digital result is the series data train at the output of the comparator.

The accuracy of this ADC is dependent on the matching of the capacitances and on the DC-gain of the amplifiers. From the quality of the amplifiers and assuming a double poly CMOS process, an overall accuracy of 16 bit can be achieved using this ADC principle. Table 7.5 shows an overview of the ADC ability based on the chopper OTA specified in chapter 6.

bit-range	accuracy	max. sample frequency	max. bandwidth
10	2.4 mV	2.6 MHz	78.4 KHz
12	610 uV	2.2 MHz	57 KHz
14	153 uV	1.9 MHz	42.3 KHz
16	38 uV	1.7 MHz	33.2 KHz

Table 7.5 Fully Differential D-VIS Incremental ADC Characteristics

7.5.2 Fully Differential D-VIS Delta-Sigma Converter

A rearrangement of the input structure of the previous presented ADC gives the fully differential D-VIS DS-ADC. Figure 7.6 shows the circuit diagram.

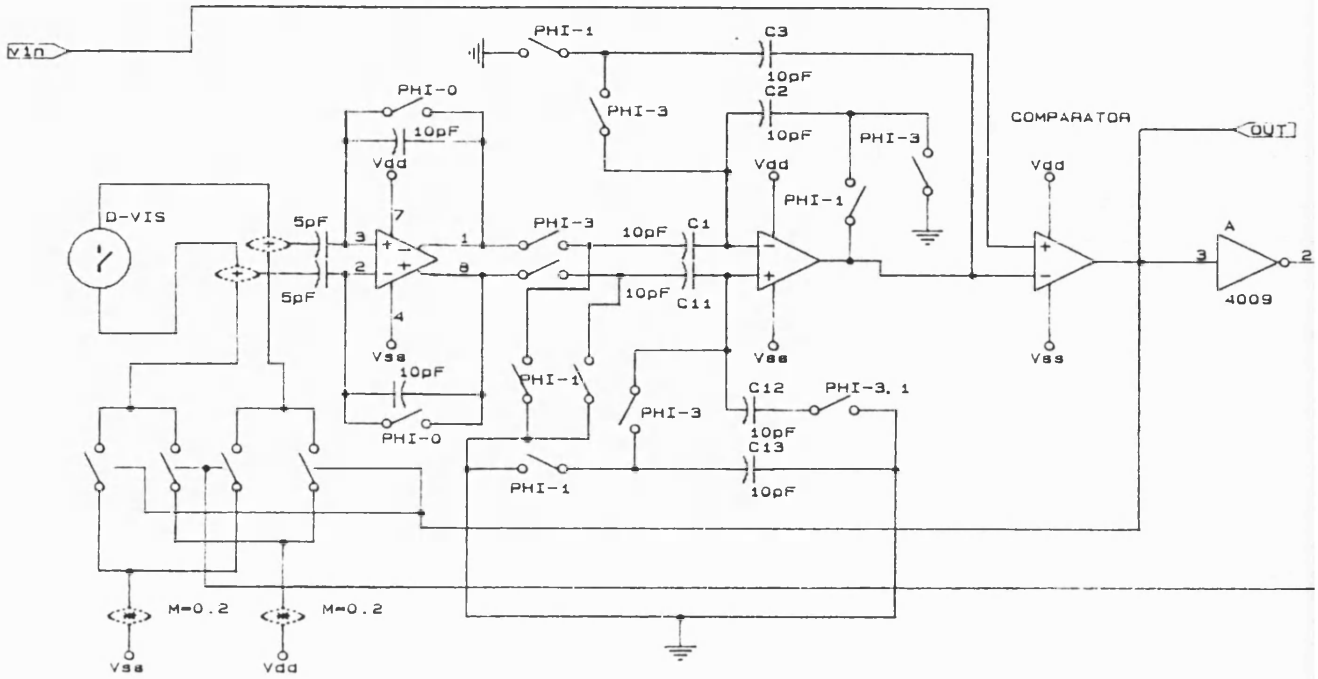

Figure 7.6 Fully Differential D-VIS Delta-Sigma ADC

The operation is comparable to that of the previous ADC. The DS-part is built with the switches and the summation at the input section of the fully differential OTA. Instead of controlling the incremental steps with the direction of the VIS outputs, the loop control is processed by switches that connect to V_{dd} or V_{ss}. The VIS output still remains at the appropriate summation nodes. The reference voltages V_{dd} and V_{ss} are scaled by a factor of 0.2 to achieve a balanced modulation and to emphasize the signal and not the correction terms. From the difference concept represented by the SD-ADC in section 7.3, the correction steps show a step by step attenuation of (Vref/2 - 0.2 V_{dd}) or (Vref/2 + 0.2 V_{ss}). By sampling the input voltage, this DS-ADC operates against a

fixed input voltage per period. Hence the oversampling factor is determined by the number of VIS-steps, to give the internal accuracy, and by the number of external s&h cycles, to give the external oversampling rate.

7.5.3 Summary of the Analogue to Digital Converter Circuits

The ADC characteristics that are realisable summarized in the following table 7.6

ADC-Type	resolution	1-bit-conv.time	fs,max	fbw	linearity
VIS SAR ADC	12 bit	1.35 usec	2.22 MHz	61.7 KHz	<0.5LSB
VIS SAR ADC (calibrated)	14 bit	1.57 usec	1.81 MHz	45.5 KHz	<0.5LSB
Alg. ADC	12 bit	1.35 usec	2.22 MHz	61.7 KHz	<0.5LSB
Alg. ADC (calibrated)	16 bit	1.77 usec	1.67 MHz	35.3 KHz	<0.5LSB
SD-ADC	10 bit	-	2.6 MHz	10 KHz	<0.5LSB
IV-SD ADC	16 bit	1.77 usec	1.67 MHz	35.3 KHz	<0.5LSB
I-D-VIS ADC	16 bit	1.77 usec	1.67 MHz	35.3 KHz	<0.5LSB
D-VIS ADC	16 bit	1.77 usec	1.67 MHz	35.3 KHz	<0.5LSB

[1] Charles, Saletore, Black, Hodges "An Algorithmic Analog-to-Digital Converter" ISSCC Dig.Tech.Papers, pp. 96-97, 1977

[2] Li P.W., Chin M.J., Gray P.R., Castello R. "A Ratio-Independent Algorithmic A/D Conversion Technique" ISSCC Dig.Tech.Papers, pp. 62-63, 1984 and IEEE, SC-19, No. 6, pp. 828-836, Dec.1984

[3] Matsumoto H., Watanabe K. "Improved Switch-Capacitor Algorithmic Analogue-to-Digital Converter" Electronics Letters, Vol. 21, No. 10, pp. 430-431, May 1985

[4] Gregorian R., Temes G.C., "Analog MOS Integrated Circuits for Signal Processing", Wiley Series, pp. 476-477, 1989

[5] Candy J.C., Benjamin "The Structure of Quantization Noise from Sigma-Delta Modulation" IEEE, COM-29, No. 9, pp. 1316-1323, Sep. 1981

[6] Robert, Temes, Valencic "A 16-BIT Low Voltage CMOS A/D Converter" IEEE, SC-22, No. 2, pp. 157-163, Apr.1987

[7] Shih C.C., Li P.W., Gray P.R. "Ratio-Independent Cyclic A/D and D/A Conversion Using a Recirculating Reference Approach" IEEE, CAS-30, No.10, pp. 772- 774, Oct. 1983

[8] Matsuya Y., Uchimura K., Iwata A., Kobayashi T., Ishikawa M., Yoshitome T., "A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping", IEEE Journal of Solid-State Circuits, Vol. SC-22, No.6, pp. 921-929, December 1987

CHAPTER 8

8. Results and Discussion

The VIS-references used for the different ADCs were simulated at a transistor level using BONSAI. Additionally, the V-VIS and the I-VIS were built on a breadboard by using a chopper amplifier with characteristics close to those of the chopper OTA. Most of the ADC circuits were simulated using the SC program. Some simulations of the ADCs were done using both BONSAI and SC to verify the SC program. BONSAI was not capable of simulating all of the A to D circuits, because of a great number of iteration errors and additionally very big simulation times (over hours up to days!). Therefore the development of the SC-program was done to be able to simulate all of the ADCs with the advantage of very low CPU times (few 10 second up to an hour).

8.1 The VIS Reference Circuits

Presented in chapter 5, the VIS reference circuits used have a more accurate reference voltage which has a stepwise divide by two characteristic. As the theoretical approach showed, the V-VIS, I-VIS and the D-VIS have very good properties. The V-VIS circuit description for the BONSAI simulation is shown in Table 8.1. The simulations were done to include parasitic capacitances. The subcircuits OTAS-TAT.TR, Widlar, CCCTR and TG_TR are shown in table 8.2.

```
.TITLE VIS - SIMULATION OF THE TRANSISTOR-CIRCUIT (OTA): OTA IN
DOUBLE USE
.TITLE W.TENTEN 15.09.1988
```

```
.INCLUDE PARM3U.BO
.INCLUDE CLOCK.ID
.INCLUDE OTASTAT.TR
.INCLUDE TG_TR

.CIRCUIT
XCL 11 111 1 101 2 102 3 103 4 104 5 105 CLOCK
$
$               PHASE 0 IS THE INITIALISATION
$               PHASE 1 IS THE MEASUREMENT
$               PHASE 2 IS THE VOLTAGE INVERSION
$               PHASE 3 IS THE CONNECTION TO NEXT STAGES (NODAL
40)
$               PHASE 3 IS THE PREPARATION OF THE VIS FOR
$                   THE NEXT CYCLE
$
XRINI 10  99 11 111 99 98 TG
XRNU1 20  60  4 104 99 98 TG
XRNU2 20   0  4 104 99 98 TG
XRNU3 60   0  4 104 99 98 TG
XRIN2 20   0 11 111 99 98 TG

XR2_2 10 20  2 102 99 98 TG
XR3_1 60  0  1 101 99 98 TG
XR3_3 60  0  3 103 99 98 TG
XR4_1 20 30  1 101 99 98 TG
XR4_3 20 30  3 103 99 98 TG
XR5_2 50 30  2 102 99 98 TG
```

```
XR6_1 40 50  1 101 99 98 TG
XR7_2 40 60  2 102 99 98 TG
$                AFTER VOLTAGE INVERSION , THE CHARGE IS
$                NOW PREPARED FOR THE NEXT STAGES AND IS
$                ADDITIONALLY PUT ONTO C10 DURING PHI 3

$    INN INZERO INP OUT BIAS KASKP KASKN VDD VSS
XMAIN1 40  90    30  40  14   15    16    99 98  OTA
XCCCM1              14   15    16    99 98  CCCTR
XWIDL1              14            99 98  WIDLAR

COUT 40 98 20

C1   10 98 50
C1T  10 98 .5
C2   20 60 50
C2T  20 98 .5
C2B  60 98 50.5
CH   50 98 50

VZERO1 90 30 125.624E-6
VDD   99 0  2.5
VSS   98 0 -2.5

.LIMIT 10000
.CHECK
ELEMENTS ALL
.OUTPUT PRINT
```

```
V(10) V(20) V(30) V(40) V(50) V(60)
V(11) V(111) V(1) V(101) V(2) V(102) V(3) V(103) V(4) V(104)
.TRAN MNA 0.25E3 0 200E3
.END
```

Table 8.1 BONSAI file of the voltage follower VIS reference circuit

```
$            IN- INZERO IN+ OUT BIAS KASKP KASKN VDD VSS
.SUBCIRCUIT OTA 20   25  30  10  40   50   60   99  98
$

$NR  D  G  S  B T  W   L  AD   AS   PD  PS
$
MP1  4  4 99 99 P 120  3  (120*13) (120*13) (120+ 2*13) (120+ 2*13)
 BONSAI V1.2c (GAMMERTINGEN 26.06.88)
   INPUT DATASET

MP2  5  5 99 99 P 120  3  (120*13) (120*13) (120+ 2*13) (120+ 2*13)
MP3  2  4 99 99 P 419  3  (419*13) (419*13) (419+ 2*13) (419+ 2*13)
MP4  8  5 99 99 P 480  3  (480*13) (480*13) (480+ 2*13) (480+ 2*13)
MP5 10 50  8 99 P 480  3  (480*13) (480*13) (480+ 2*13) (480+ 2*13)
MN1  4 20  7  7 N 250  3  (250*13) (250*13) (250+ 2*13) (250+ 2*13)
MN2  5 30  7  7 N 250  3  (250*13) (250*13) (250+ 2*13) (250+ 2*13)
MN3  7 40 98 98 N  80  9  ( 80*13) ( 80*13) ( 80+ 2*13) ( 80+ 2*13)
MN4  2  2 98 98 N 140  3  (140*13) (140*13) (140+ 2*13) (140+ 2*13)
MN5  9  2 98 98 N 140  3  (140*13) (140*13) (140+ 2*13) (140+ 2*13)
MN6 10 60  9 98 N 140  3  (140*13) (140*13) (140+ 2*13) (140+ 2*13)
$
```

```
$ ADDITIONAL INPUT STAGE FOR THE NULLING SECTION
$
MN10  4 25 17 17 N 125  3  (125*13) (125*13) (125+ 2*13) (125+ 2*13)
MN11  5 30 17 17 N 125  3  (125*13) (125*13) (125+ 2*13) (125+ 2*13)
MN12 17 40 98 98 N  40  9  ( 40*13) ( 40*13) ( 40+ 2*13) ( 40+ 2*13)
$              BIAS VDD VSS
.SUBCIRCUIT WIDLAR 1    99  98
MP1  2  2 99 99 P  36  9  ( 36*13) ( 36*13) ( 36+ 2*13) ( 36+ 2*13)
MP2  1  2 99 99 P  36  9  ( 36*13) ( 36*13) ( 36+ 2*13) ( 36+ 2*13)
MN1  2  1  3  3 N 144  9  (144*13) (144*13) (144+ 2*13) (144+ 2*13)
MN2  1  1 98 98 N  16  9  ( 16*13) ( 16*13) ( 16+ 2*13) ( 16+ 2*13)
R1 3 98 16
$              BIAS KASKP KASKN VDD VSS
.SUBCIRCUIT CCCTR    40   4    2    99  98
MP1  2  1 99 99 P 114  3  (114*13) (114*13) (114+ 2*13) (114+ 2*13)
MP2  1  1 99 99 P 114  3  (114*13) (114*13) (114+ 2*13) (114+ 2*13)
MP3  4  4  1 99 P 114  3  (114*13) (114*13) (114+ 2*13) (114+ 2*13)
MN1  2  2  3 98 N  80  3  ( 80*13) ( 80*13) ( 80+ 2*13) ( 80+ 2*13)
MN2  3  3 98 98 N  80  3  ( 80*13) ( 80*13) ( 80+ 2*13) ( 80+ 2*13)
MN3  4 40 98 98 N  48  9  ( 48*13) ( 48*13) ( 48+ 2*13) ( 48+ 2*13)


$          IN OUT PHI1 PHI1N VDD VSS
.SUBCIRCUIT TG 10 20  100  110   99 98
MP1 10 110 20 99 P 3 3 (3*13) (3*13) (3 + 2*13) (3 + 2*13)
MN1 10 100 20 98 N 3 3 (3*13) (3*13) (3 + 2*13) (3 + 2*13)
```

Table 8.2 BONSAI transistor level description of the building blocks

Figure 8.1 shows the BONSAI simulated results. This plot shows the voltage across the input capacitance and the voltage while the output phase is active (phase 3). Figure 8.2 shows a series of photographs of the waveforms from the breadboard V-VIS. The breadboard circuits are buildt using a chopper amplifier with characteristics close to the chopper amplifier presented in section 3.3.3.2. The CMOS switches are CD4066 circuits. The photos show in detail:

Figure 8.2 a: The overall staircase of the V-VIS for a 10-bit resolution.

Figure 8.2.b: The step 3.125V is highlighted and measured by the oscilloscope.

Figure 8.2.c: The step 2.8125V is highlighted and measured by the oscilloscope.

Figure 8.2.d: The step 2.500V is highlighted and measured by the oscilloscope

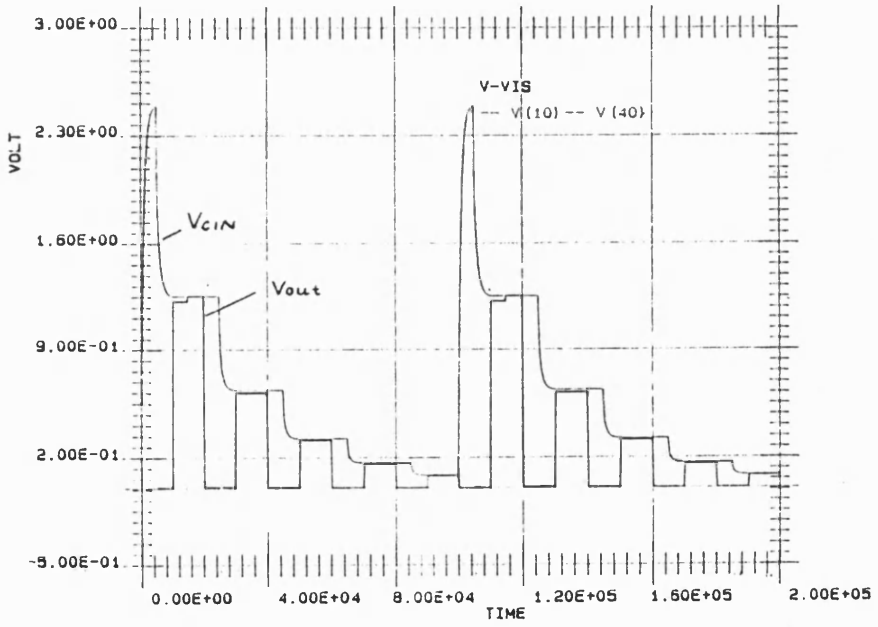

Figure 8.1 Voltage follower VIS reference circuit BONSAI simulation

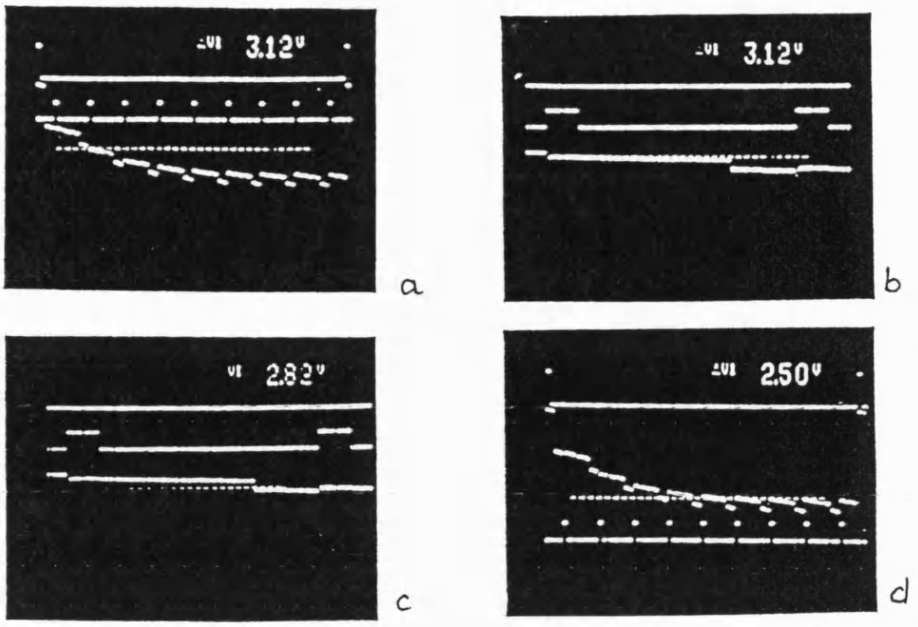

Figure 8.2 Photo series of the V-VIS breadboard

The breaks in between the different steps are due to the very large parasitic capacitances of the breadboard VIS circuit. The VIS measures all of these leakages and must refresh its final voltage with the measured error voltage. The two peaks at the top of figure 8.2a are the start of conversion signal. Each start of conversion signal also shows that the previous cycle is finished, and the digital word is complete. The second waveform is the clock PHI-3. This is the time during which the ADC step is completed.

The I-VIS BONSAI description is shown in Table 8.3

.TITLE INTEGRATOR VIS - SIMULATION OF THE TRANSISTORIZED-CIR-CUIT

.TITLE W.TENTEN 29.12.1988

```
.INCLUDE PARM3U.BO
.INCLUDE CLOCK.ID
.INCLUDE OTASTAT.TR
.INCLUDE TG_TR

.CIRCUIT

XCLOCK 11 111 1 101 2 102 3 103 4 104 5 105 CLOCK

X:R0   99 10 11 111 99 98 TG
X:R1_3  10 20  3 103 99 98 TG
X:R2_1  30 40  1 101 99 98 TG
X:R2_2  30 40  2 102 99 98 TG
X:R3_3  60 30  3 103 99 98 TG
X:R4_1  60 40  1 101 99 98 TG
X:R5_1   0 20  1 101 99 98 TG
X:R5_2   0 20  2 102 99 98 TG

X:R5_4   0 20  4 104 99 98 TG
X:R2_4  30 40  4 104 99 98 TG
$      INN INZ INP OUT BIAS KASKP KASKN VDD VSS
XOTAVIS 40  97  0   60  150  16    17    99  98 OTA
XCCCVIS              150  16    17    99  98 CCCTR

XWID1                150           99  98 WIDLAR

C0    10 98 20
CT0   10 98 0.2
```

```
C1   20 30 20
CT1  20 98 0.2
CB1  30 98 20.2
CI   40 60 20
CTI  40 98 0.2
CBI  60 98 20.2

VINZ1  96  0  125E-6
VINZ2  97  0  125E-6
VDD    99  0  2.5
VSS    98  0 -2.5

.LIMIT 10000
.OUTPUT PRINT
V(10) V(20) V(30) V(40) V(60)
V(1) V(2) V(3) V(4) V(5)
V(150) V(16) V(17)
.TRAN MNA .25E3 0 200E3
.END
```

Table 8.3 BONSAI file of the Integrator VIS reference circuit

Figure 8.3 shows the plot of a BONSAI simulation of the I-VIS. The simulations include parasitic capacitances. This plot shows the output node during phase three. The update to Vdd was not included in this simulation and no load capacitance was connected to the output node. Therefore the plot shows just the division by two results. This plot shows the ideal operation of the VIS without the influence of a clock-feed through reaction. The voltage range for this simulation was balanced between Vdd=2.5V and Vss=-2.5V.

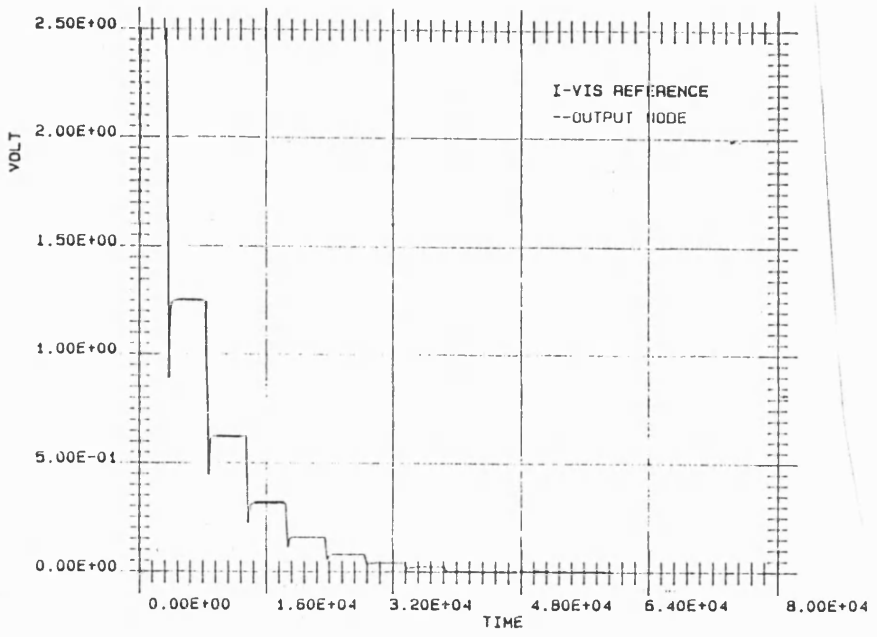

Figure 8.4 I-VIS reference circuit simulated with BONSAI

This circuit was built on a breadboard by using a chopper amplifier of comparable characteristics to those of the OTA presented in chapter 6. Figure 8.5 shows a sequence of photographs. The overall accuracy of this I-VIS was 10 bit. The photos show in detail:

Figure 8.5a: The staircase of the I-VIS and the measured 1.250V line.

Figure 8.5b: The staircase of the I-VIS and the measured 0.625V line.

Figure 8.5c: The staircase of the I-VIS and the measured 0.3125V line.

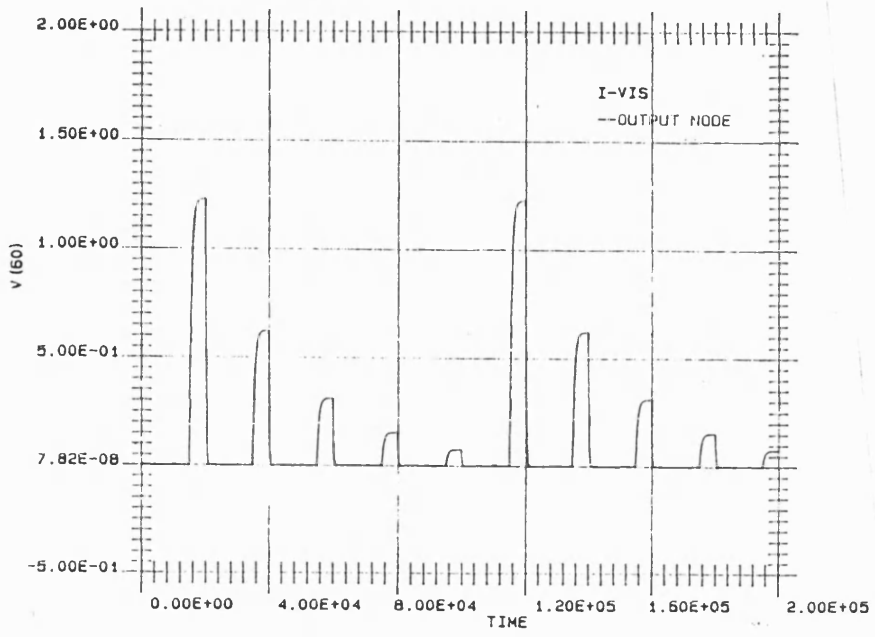

Figure 8.3 I-VIS BONSAI simulation

Figure 8.4 shows the "real" I-VIS circuit result with a load capacitance at the I-VIS output. The clock feed through spikes are visible. The simulation result show an accuracy of 16 bit including the parasitic effects.

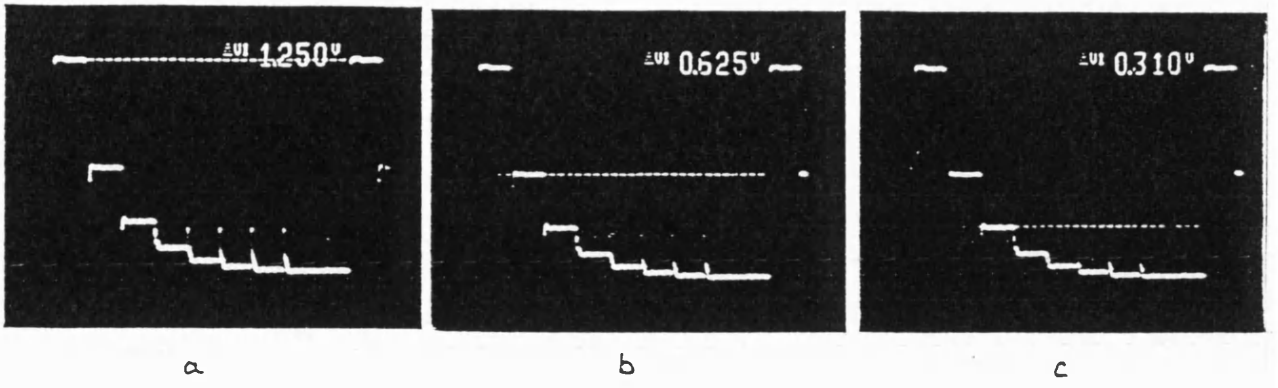

Figure 8.5 Photo series of the I-VIS breadboard

The spikes are due to clock-feed through. The clock control signals are not included in this photo series, because they are the same as in the V-VIS photos. BONSAI results and measured results show very good agreement. The matching error is below the 0.5LSB termination. Hence the technique used to simulate the VIS circuits and to simulate the ADCs is verified.

The fully differential VIS (D-VIS) was simulated using voltage controlled voltage sources (VCVS). This simulation was verified by some simulations of the V-VIS and I-VIS with VCVS. These results show perfect agreement, so the simulation of the D-VIS is very accurate. Figure 8.6 shows the BONSAI simulation of the fully differential VIS reference.

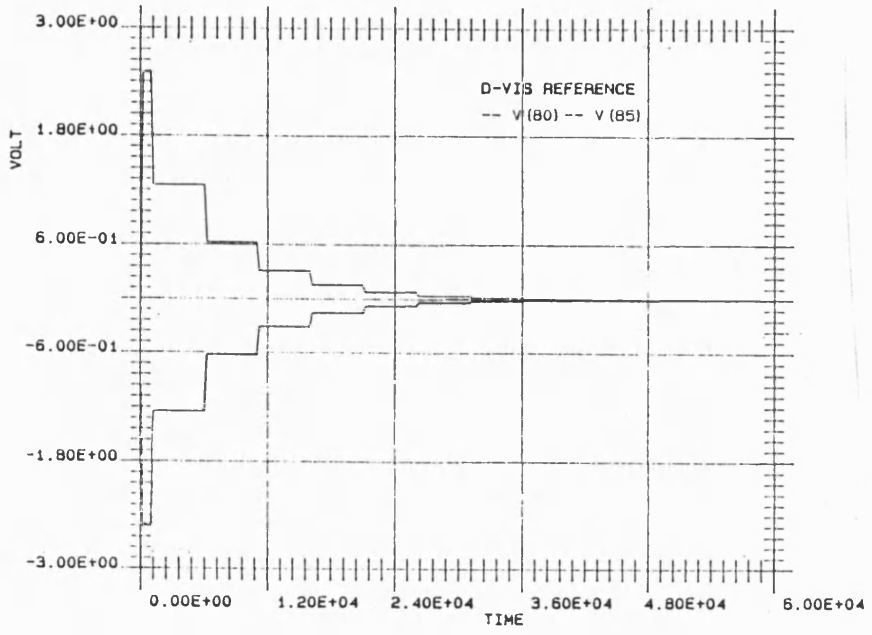

Figure 8.6 Fully-differential VIS reference circuit simulated with BONSAI

8.2 Simulation Results of the Analogue to Digital Converter

Firstly the simulated results of the successive approximation ADC (SA-ADC) will be presented. The first set of simulations was done with BONSAI. The second set of simulation was done with the SC-program. The following list shows the organisation of the plots to verify the SA-ADC.

Figure 8.7 BONSAI simulation Vin=0.05V

Figure 8.8 BONSAI simulation Vin=3.00V

Figure 8.9 BONSAI simulation Vin=4.96V

Figure 8.10 SC simulation Vin=0.05V

Figure 8.11 SC simulation Vin=2.4V

It is to noted, that the simulation with BONSAI uses V_{dd}=5V and V_{ss}=0V, but the SC simulations were done using as the supply voltages the balanced condition +/- 2.5V.

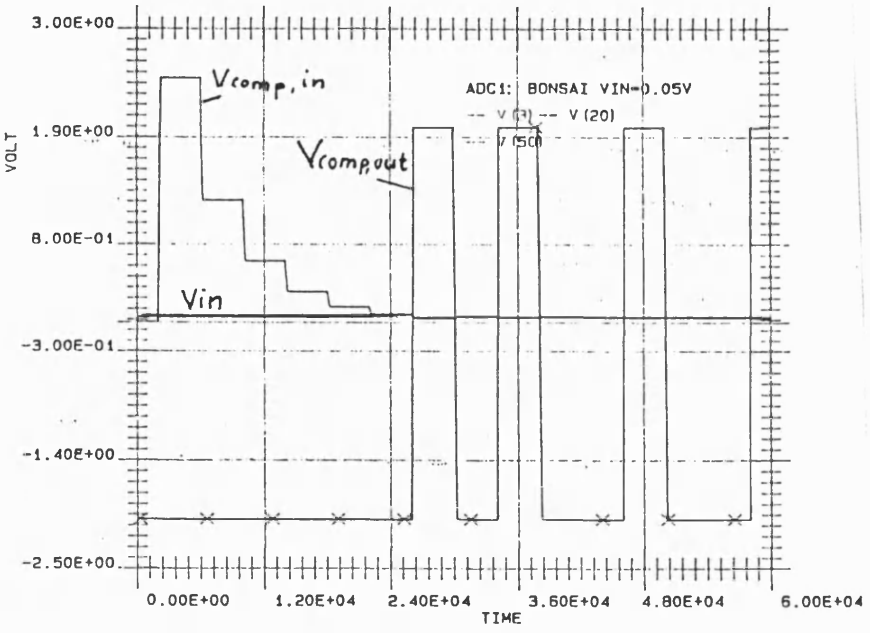

Figure 8.7 SA-ADC BONSAI simulation Vin=0.05V

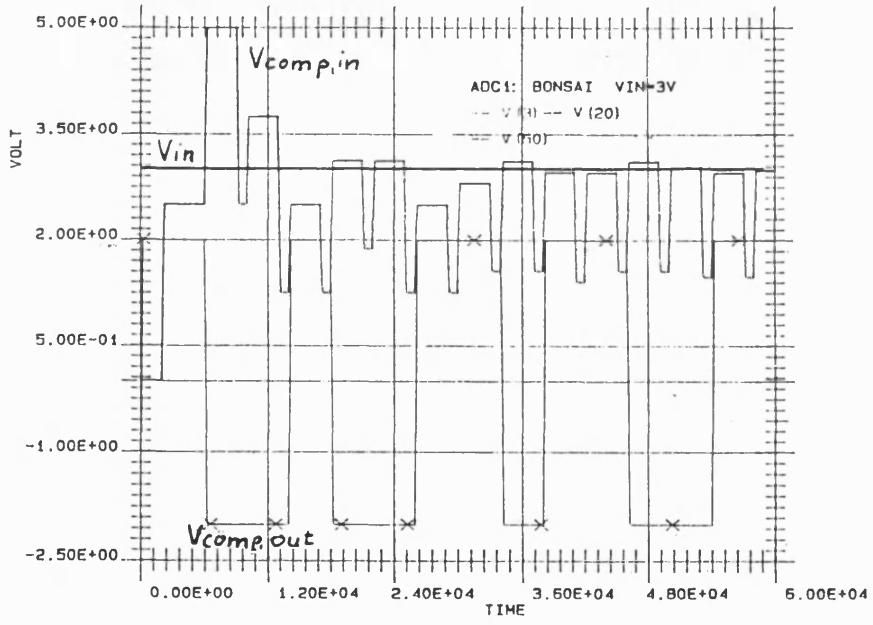

Figure 8.8 SA-ADC BONSAI simulation Vin=3V

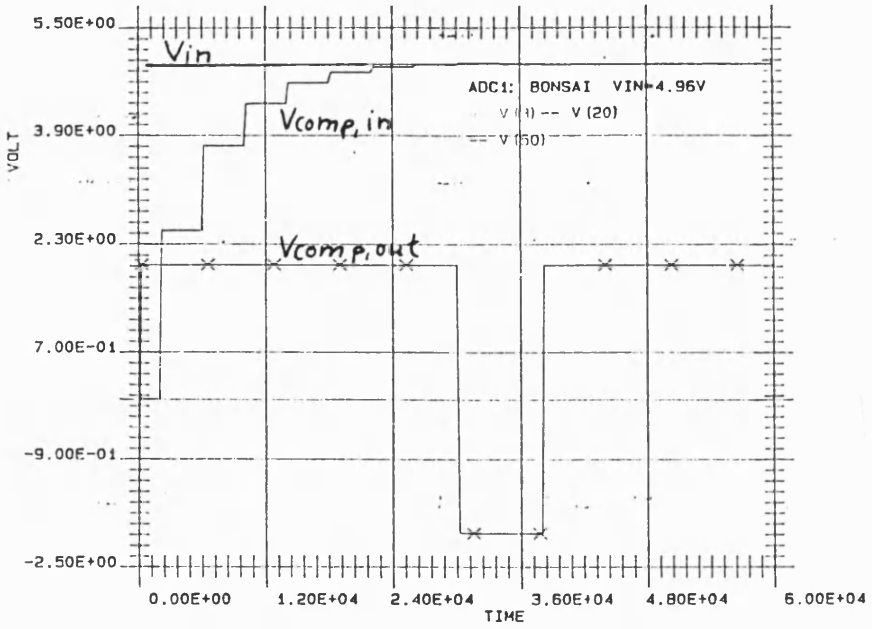

Figure 8.9 SA-ADC BONSAI simulation Vin=4.96V

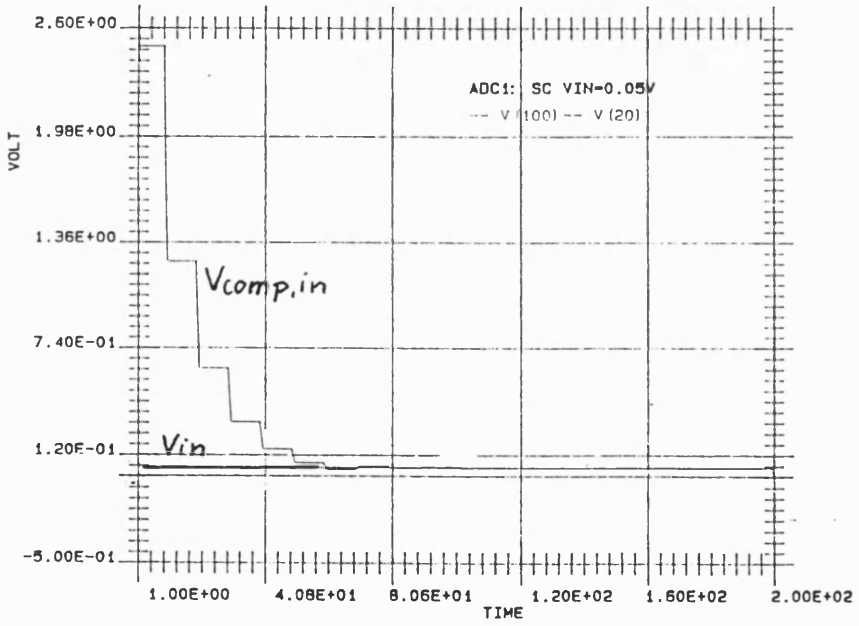

Figure 8.10 SA-ADC SC simulation Vin=0.05V

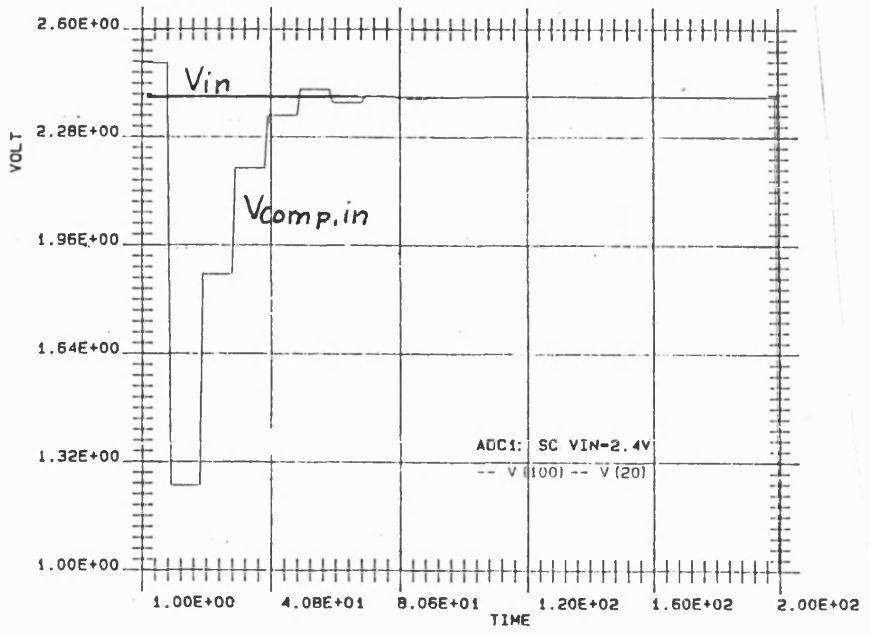

Figure 8.11 SA-ADC SC simulation Vin=2.40V

The simulation show a proper response of the SA-ADC under control of the VIS. The simulated accuracy, if the elements show an offset of 0.5mV and clock feed-through, is better than 10 bit. So a minimum resolution of 10 bit is realistically achievable. Due to the 2-capacitor array, in which the VIS control loop is included, the linearity is better than 0.5LSB.

8.3 Simulated Results of the Algorithmic ADC

The algorithmic ADC is simulated using BONSAI and SC. The following simulations were done to verify the design:

Figure 8.12 BONSAI simulation Vin=1.014V

Figure 8.13 BONSAI simulation Vin=3.00V

Figure 8.14 BONSAI simulation Vin=4.999V

Figure 8.15 SC Vin=3V

Figure 8.16 SC Vin=2.455V

Figure 8.17 SC Vin=1.014V

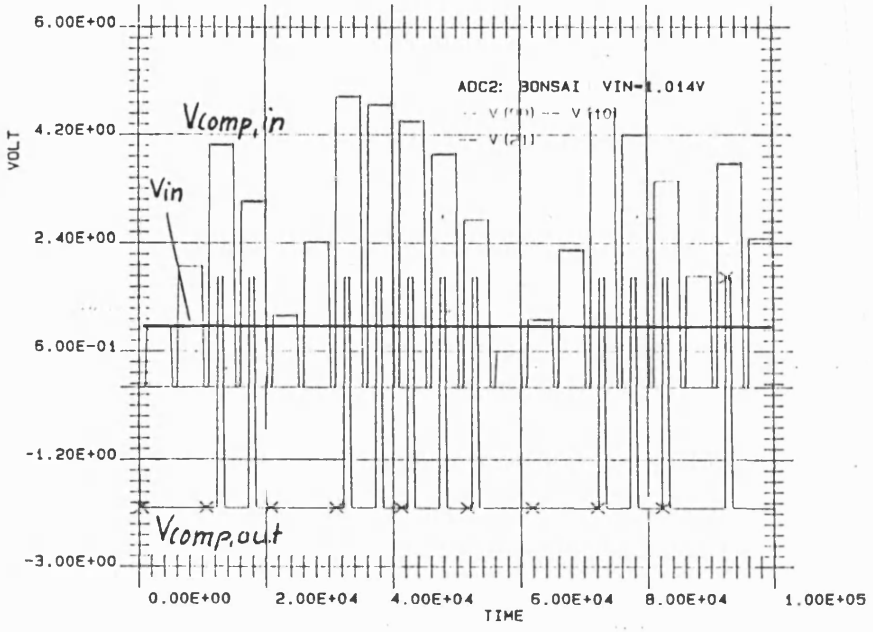

Figure 8.12 BONSAI simulation Vin=1.014V

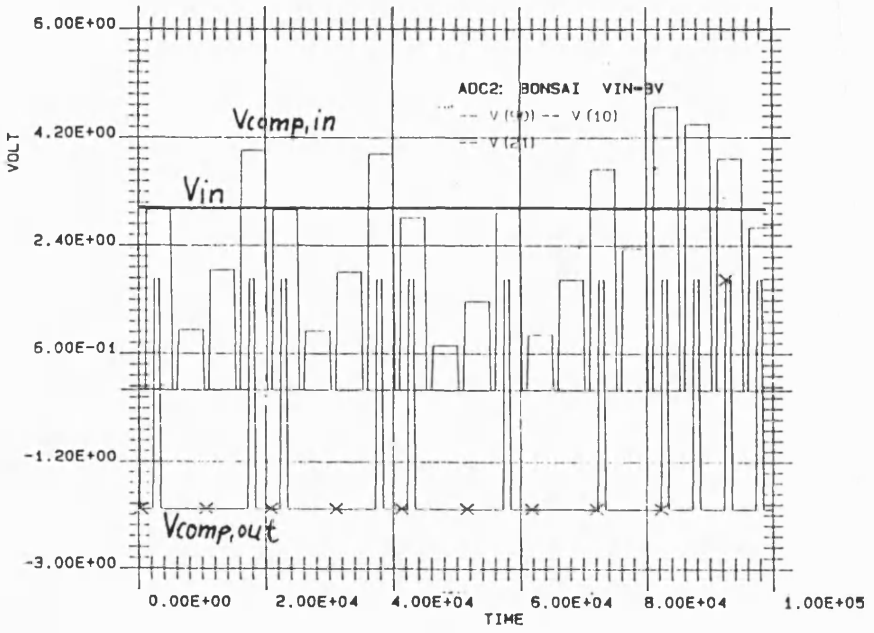

Figure 8.13 BONSAI simulation Vin=3.00V

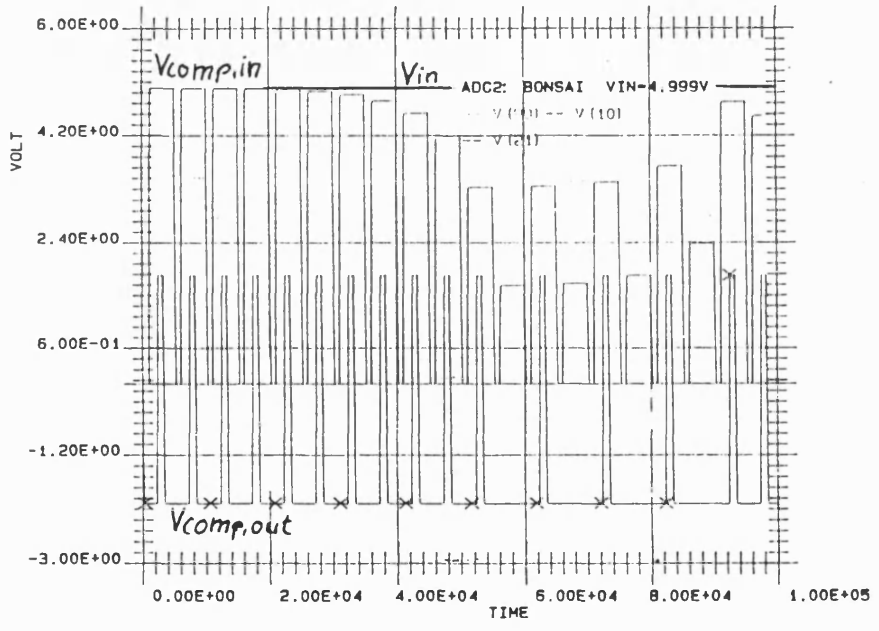

Figure 8.14 BONSAI simulation Vin=4.999V

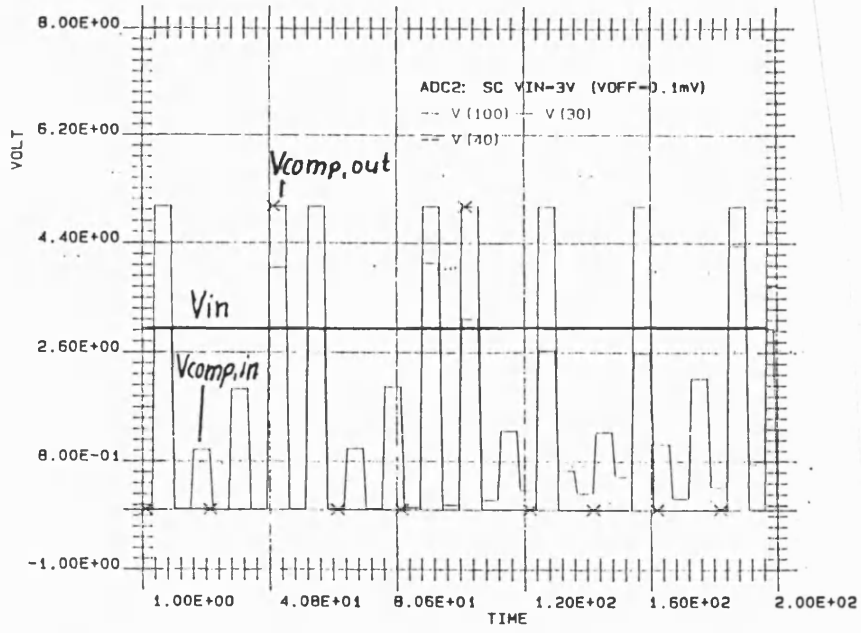

Figure 8.15 SC simulation Vin=3.00V

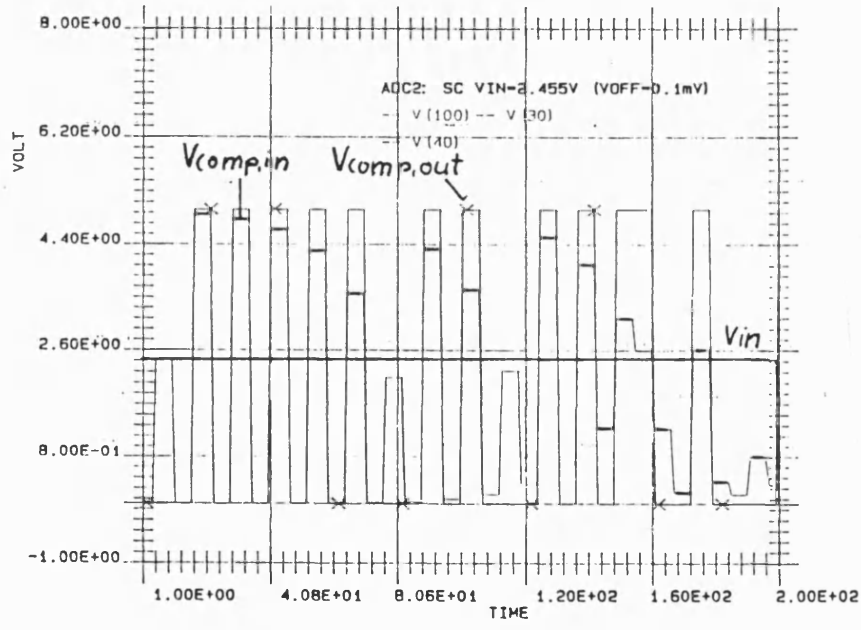

Figure 8.16 SC simulation Vin=2.455V

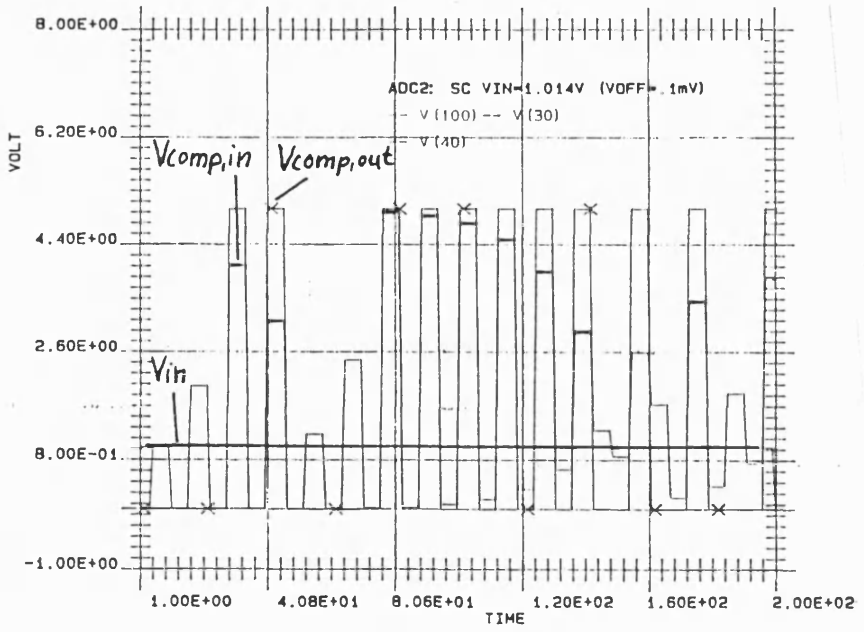

Figure 8.17 SC simulation Vin=1.014V

The results of the plots above are tabulated as:

simulation	Voltage	binary word (17digits)	voltage	accuracy
BONSAI	1.014V	0 0 1 1 0 0 1 1 1 1 1 0 0 0 1 1 1	1.0134506V	0.99945
BONSAI	3.000V	1 0 0 1 1 0 0 1 1 0 0 1 0 0 1 0 1	2.9994965V	0.99983
BONSAI	4.999V	1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1	4.9983597V	0.99987
SC	3.000V	1 0 0 1 1 0 0 1 1 0 1 0 0 1 0 0 1	3.0000832V	1.00028

SC	2.455V	0 1 1 1 1 1 0 1 1 0 1 1 1 0 1 0 0	2.4555969V	1.00024
SC	1.014V	0 0 1 1 0 0 1 1 1 1 1 1 0 1 0 1 0	1.0147858V	1.00077

The simulation results show an accuracy in the range of 10 bit. The SC-simulation with an internal amplifier offset of 0.1mV and 1mV comparator hysteresis are also within the error limits.

8.4 Difference Delta-Sigma ADC

The difference ADC was simulated with BONSAI and SC. BONSAI was just able to show a few steps of this ADC within the acceptable CPU time used for the simulation runs. The SC simulator was used to create results over a big data range. The following simulation arrangement is presented:

Figure 8.18 BONSAI Vin = 2.0155V

Figure 8.19 BONSAI Vin = 0.012V

Figure 8.20 SC Vin = 2.3V

Figure 8.21 SC Vin = -2.3V

Figure 8.22 SC Vin = sine wave 2.5V Fin=6.4kHz Fsample=2MHz

Figure 8.23 SC FFT plot integrator output

Figure 8.24 SC FFT plot comparator output

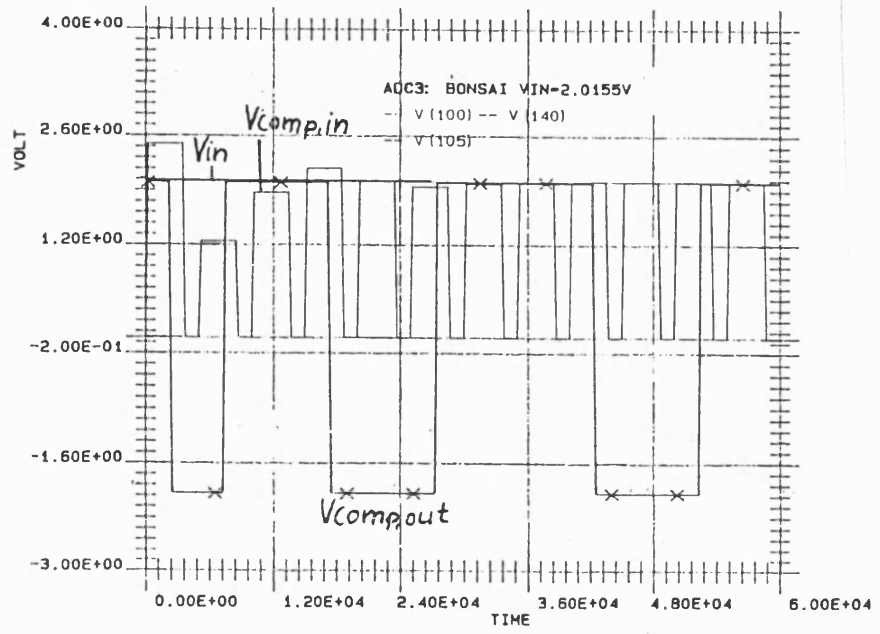

Figure 8.18 Difference SD-ADC BONSAI simulation Vin = 2.0155V

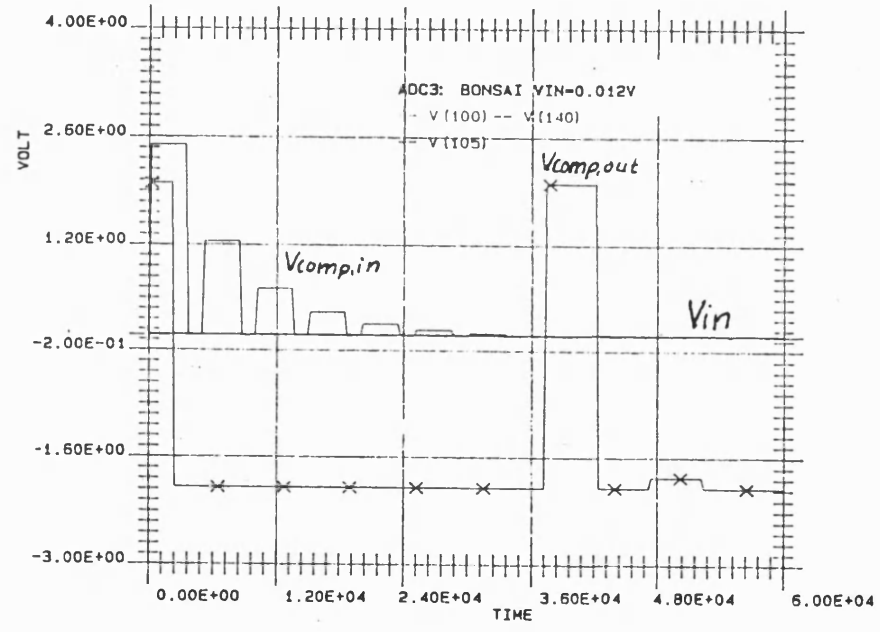

Figure 8.19 Difference SD-ADC BONSAI simulation Vin = 0.012V

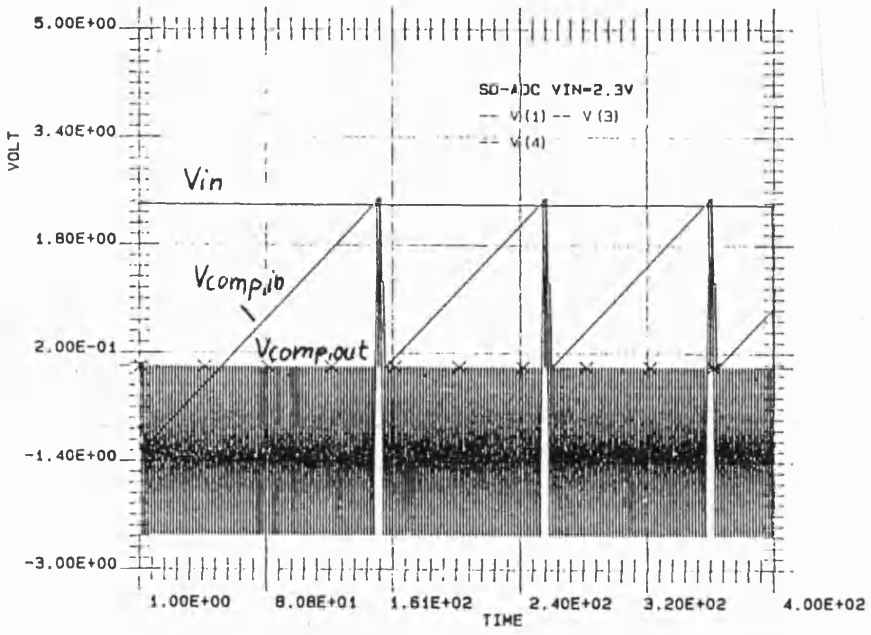

Figure 8.20 Difference SD-ADC SC simulation Vin = 2.3V

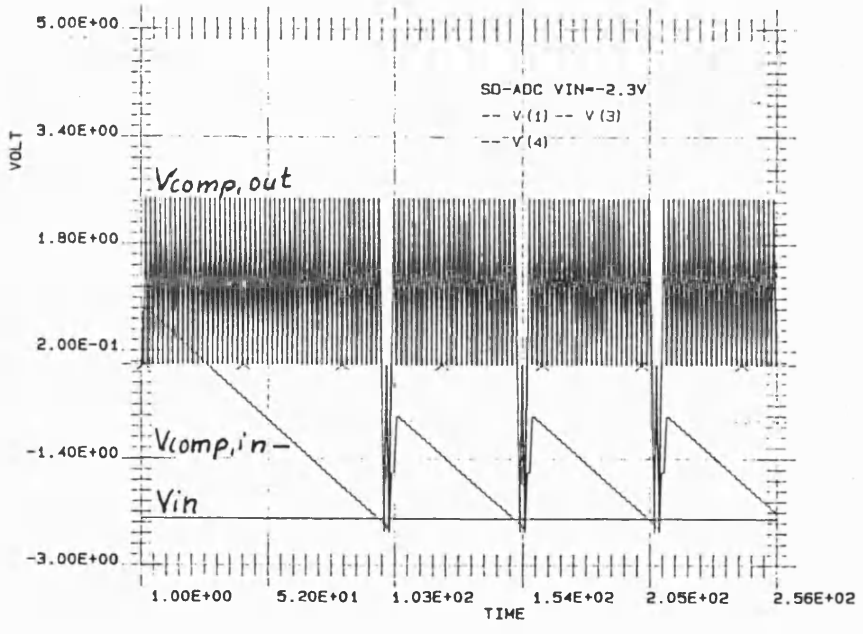

Figure 8.21 Difference SD-ADC SC simulation Vin = -2.3V

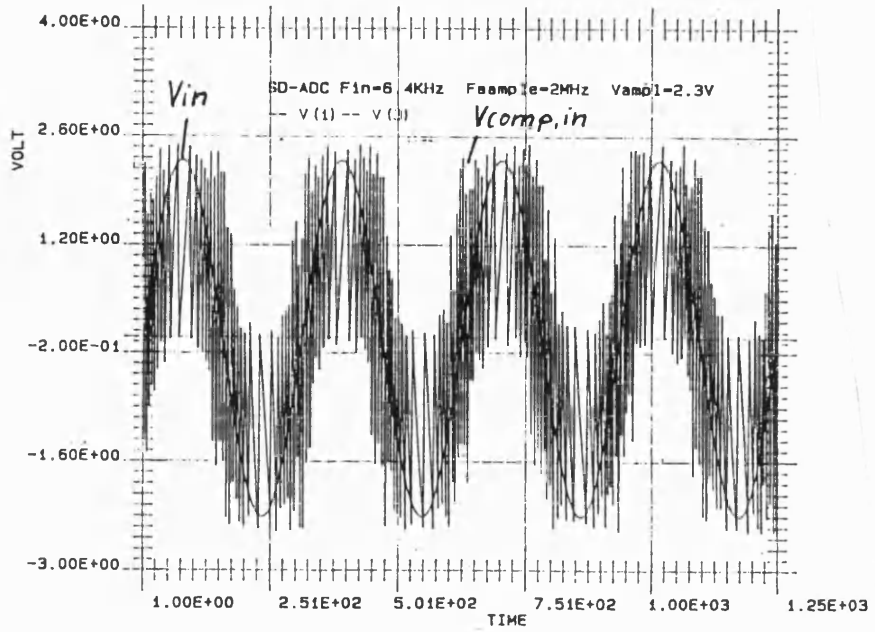

Figure 8.22 Difference SD-ADC SC simulation sinusoidal input

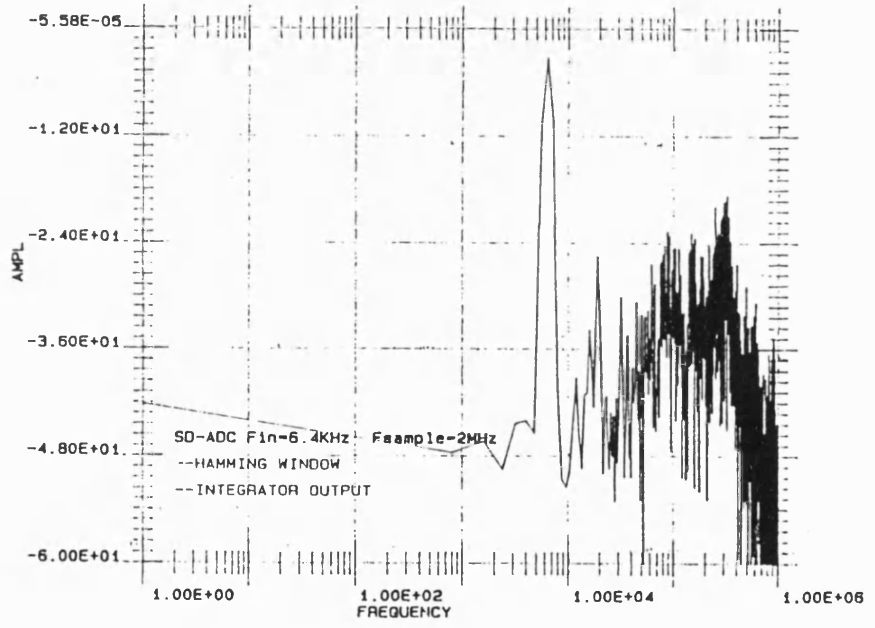

Figure 8.23 Difference SD-ADC FFT analysis integrator output

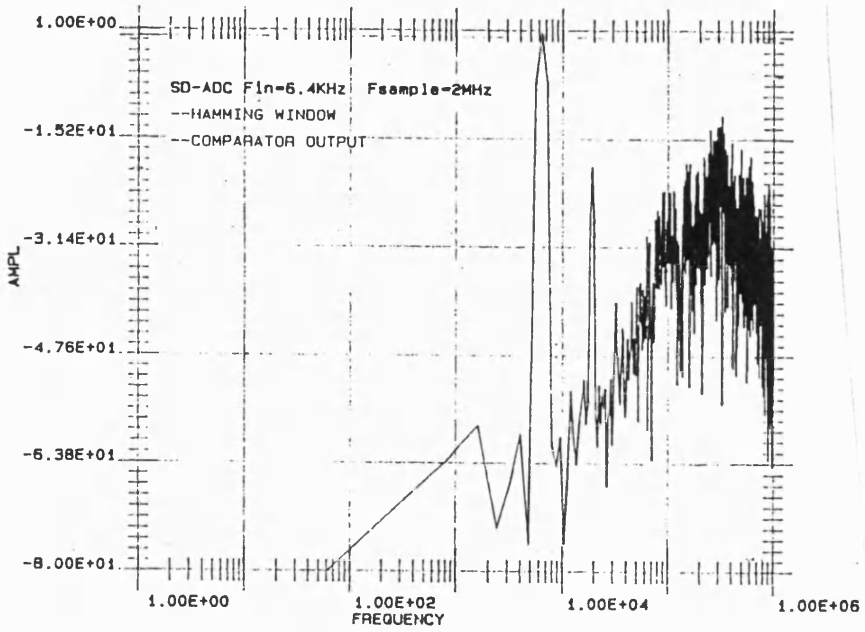

Figure 8.24 Difference SD-ADC FFT analysis comparator output

The simulation results in figures 8.18 to 8.21 show the response of the circuit for 1 ADC step. The input signal remains constant throughout this interval. Therefore the result can be evaluated to 16 bit accuracy. The input signal is slewing over this interval, and the simulation of figure 8.23 shows this situation. The overall accuracy must therefore be spilt into the following conditions: If the signal is stable over the period used to handle 16 bit with 0.5LSB resolution, the circuit acts with the full resolution. But operating this circuit as the conventional delta sigma converter, the accuracy is limited to about 8 bit. The appropriate FFT results improve the theoretical value of the signal to noise ratio (SNR) of -56.56dB within signal bandwidth of about 10kHz to -73.2dB.

8.5 Incremental VIS Controlled Delta-Sigma ADC

The incremental VIS controlled DS-ADC (IV-SD-ADC) simulation uses the SC program. The following simulation were selected:

Figure 8.25 Vin = 0V to -2.4V

Figure 8.26 Vin = 2.45V to 0V

Figure 8.27 Vin = sine-wave Amplitude = 2.5V

Figure 8.28 Fin=8.016kHz sine-wave

Figure 8.29 Zoom view of figure 8.28 inclusively the comparator output

Figure 8.30 FFT result of the s&h stage output node

Figure 8.31 FFT result of the comparator input node

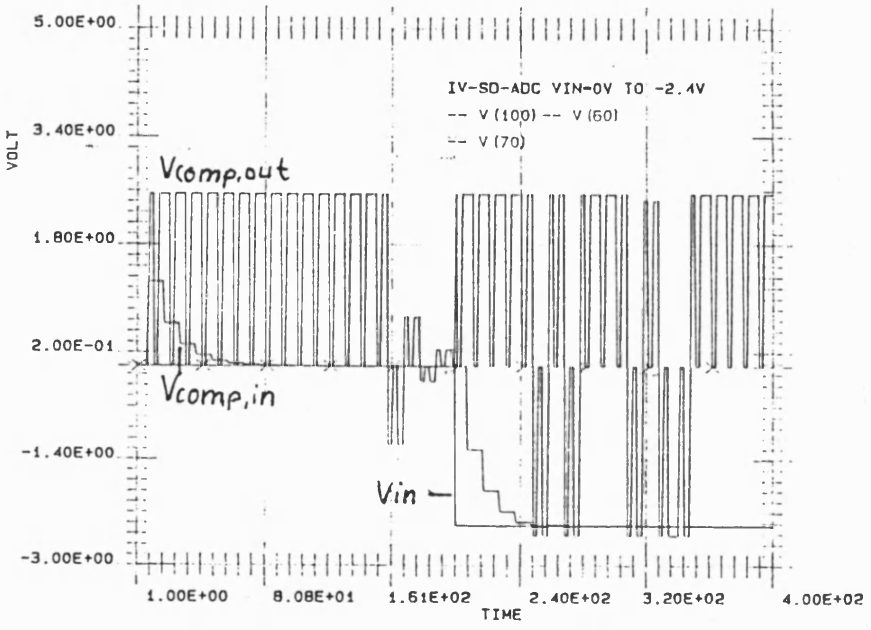

Figure 8.25 IV-SD-ADC Vin = 0V to -2.4V

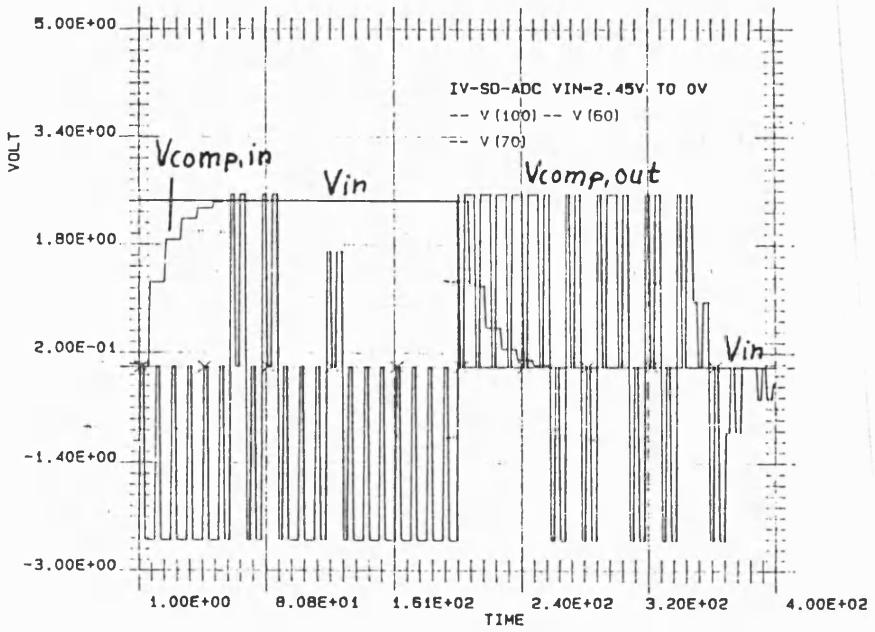

Figure 8.26 IV-SD-ADC Vin = 2.45V to 0V

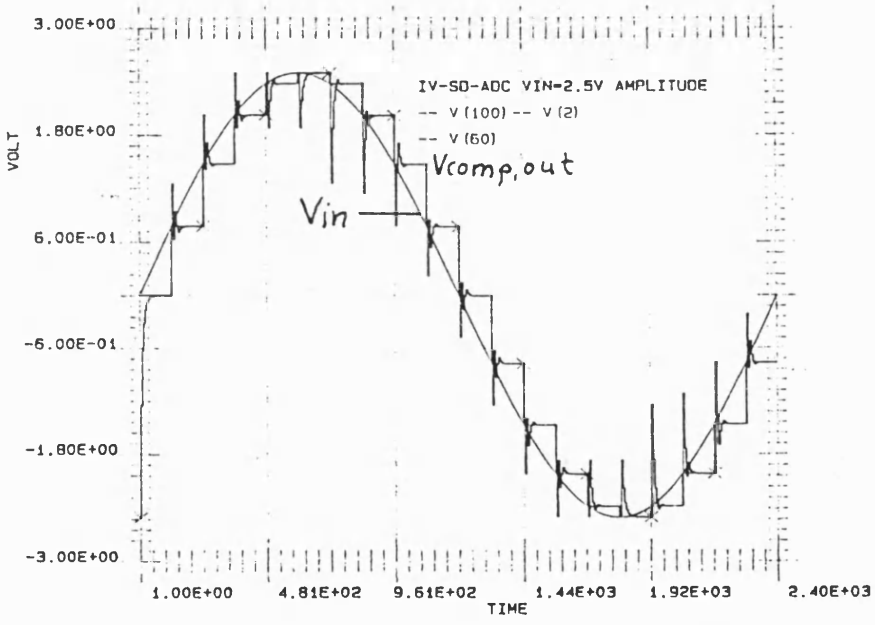

Figure 8.27 IV-SD-ADC Vin = sine-wave with amplitude 2.5V

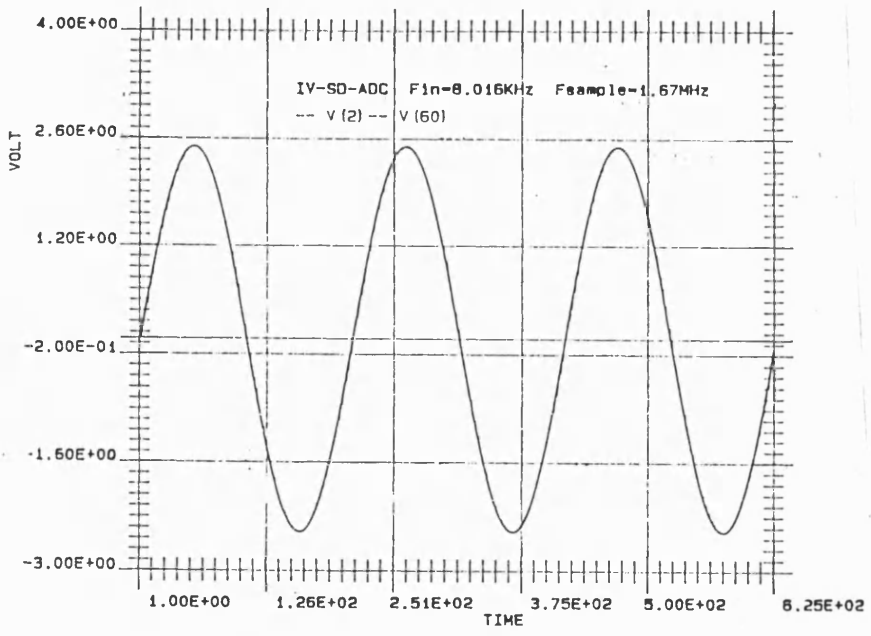

Figure 8.28 IV-SD-ADC Fin=8.016kHz Fsample=1.67MHz

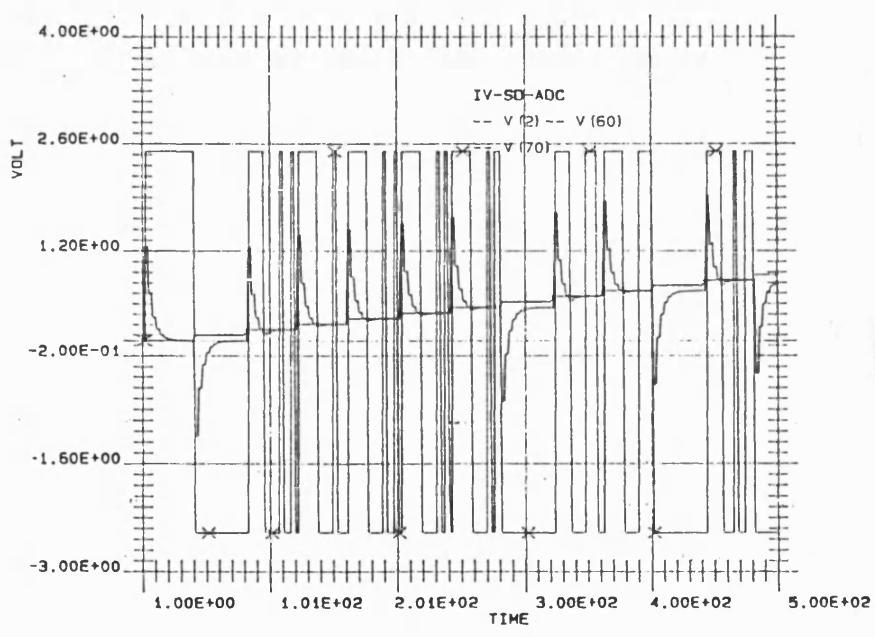

Figure 8.29 IV-SD-ADC Zoom-view of figure 8.28

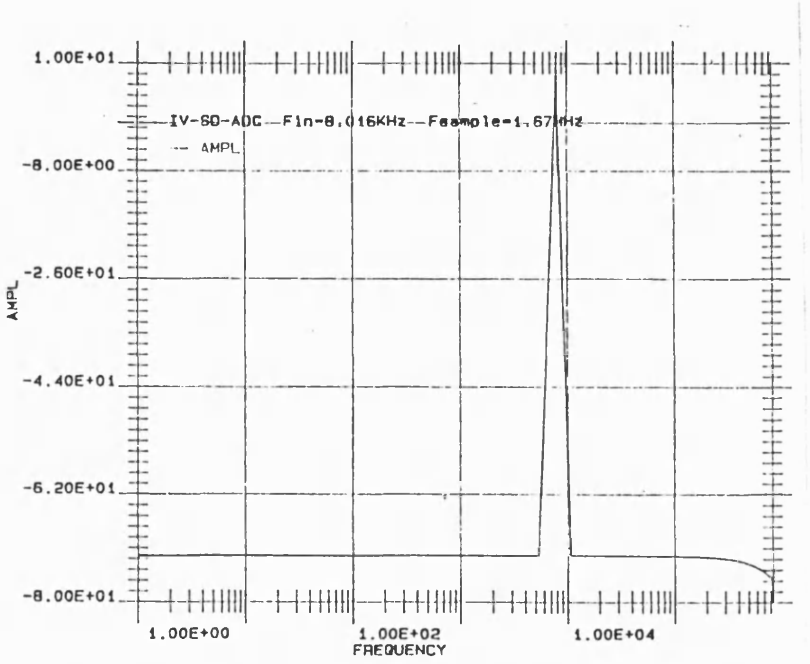

Figure 8.30 IV-SD-ADC FFT result of the s&h stage output node

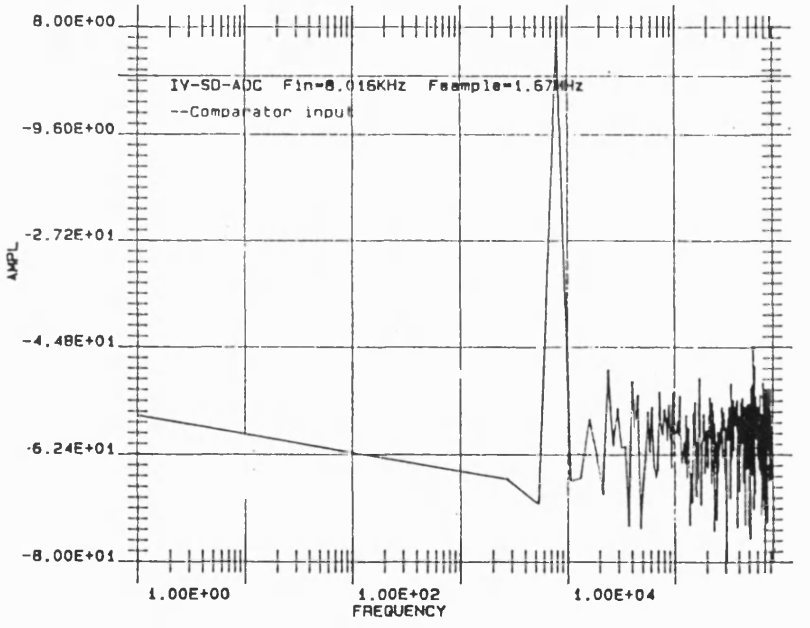

Figure 8.31 IV-SD-ADC FFT result of the comparator input node

The incremental operation under control of a VIS circuit offers the possibility of building an A to D converter with improved quality. The design presented here was simulated using more than 18 bit in figures 8.25 and 8.26. Figure 8.27 was simulated by using an internal accuracy of 16 bit, the other figures were simulated by using a 12

bit resolution. The expected SNR of a sine wave sampled with 12 bit accuracy is 74dB. The FFT result shows the expected damping within the passband, that is about 30 kHz. The theoretical passband shown in the previous section is dependent on the accuracy. Using 12 bit accuracy, the expected passband is about 47kHz. The in-band noise within 47kHz shows an increase of about 20dB. Hence the passband is also limited by the noise produced by the samples. The computed SNR of the spectrum in figure 8.31 is 81.6dB.

8.6 Fully Differential VIS Controlled Incremental ADC

The simulations of this ADC were:

Figure 8.32 Vin = 1.2V

Figure 8.33 Vin = -1.2V

Figure 8.34 Vin = 2.45V TO -1.2V

Figure 8.35 Vin = -2.4999V TO -1.245V

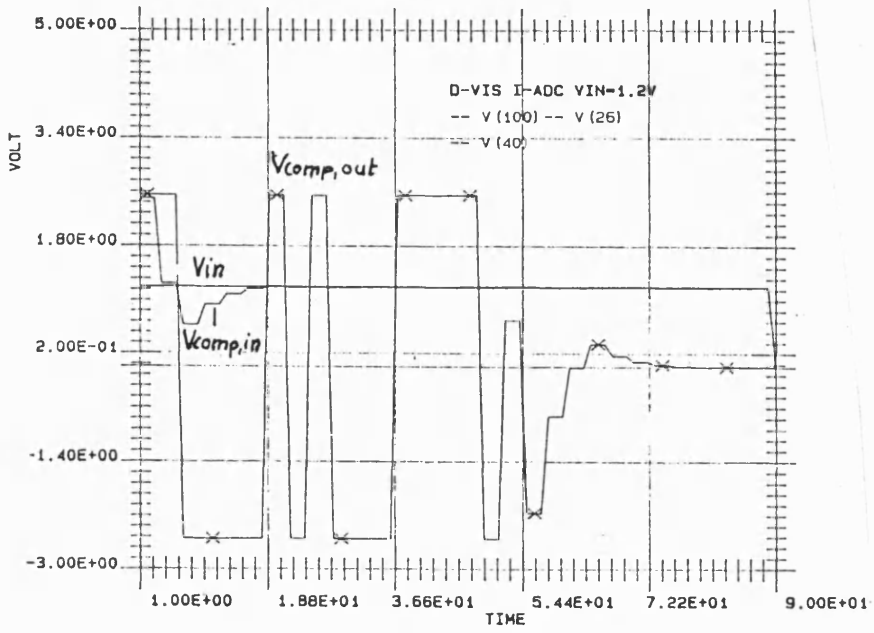

Figure 8.32 D-VIS I-ADC Vin = 1.2V

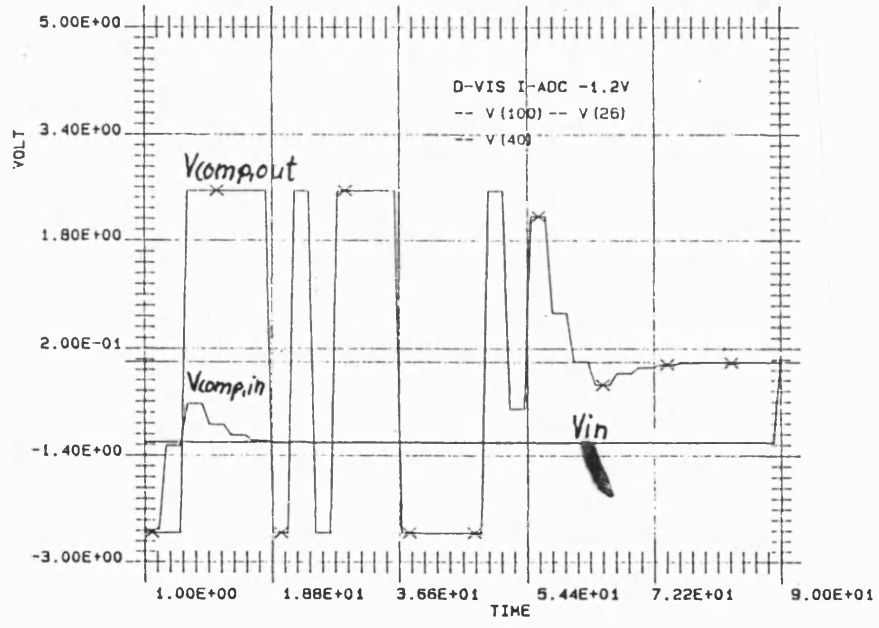

Figure 8.33 D-VIS I-ADC Vin = -1.2V

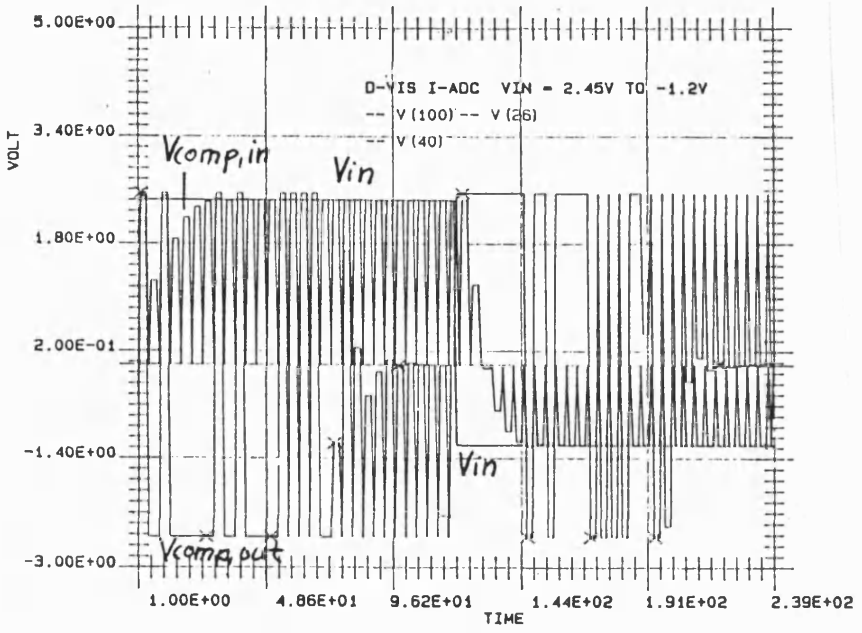

Figure 8.34 D-VIS I-ADC Vin = 2.45V TO -1.2V

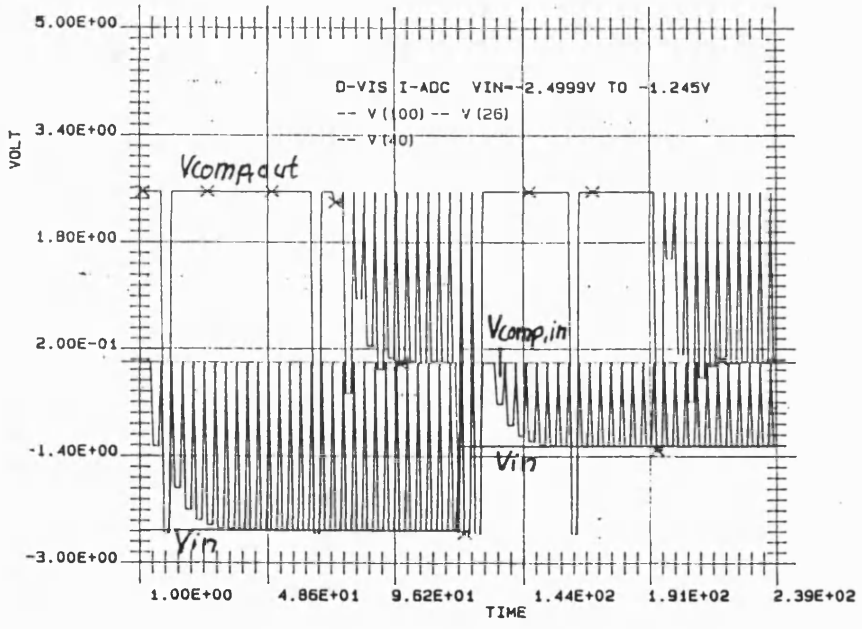

Figure 8.35 D-VIS I-ADC Vin = -2.499V TO -1.245VV

The simulations were done with more than 18 bit accuracy. Beyond the 18th bit, the accuracy is getting worse. This is because of the finite gain of the amplifiers. The digital output is evaluated thus:

Digit = HIGH: The analogue value is stored with a positive sign.
Digit = LOW: The analogue value is stored with a negative sign.

The digital output information of the plots above shows an inverted logic. The logic control of this ADC can easily arranged (see chapter 7.5.1).

8.7 Fully Differential Delta Sigma ADC

The last new ADC design proposed is based on the ADC of the last section. The performance of the fully differential delta sigma ADC (D-VIS SD-ADC) is shown in the following plots created with the SC program:

Figure 8.36 Vin = 0V
Figure 8.37 Vin = 2.0V
Figure 8.38 Vin = 1.2V
Figure 8.39 Vin = -2.4V
Figure 8.40 Vin = sine wave with Fin = 594Hz Fsample = 1.67MHz
Figure 8.41 Zoom from figure 8.40
Figure 8.42 FFT result of the sine-wave with Fin = 4.9kHz

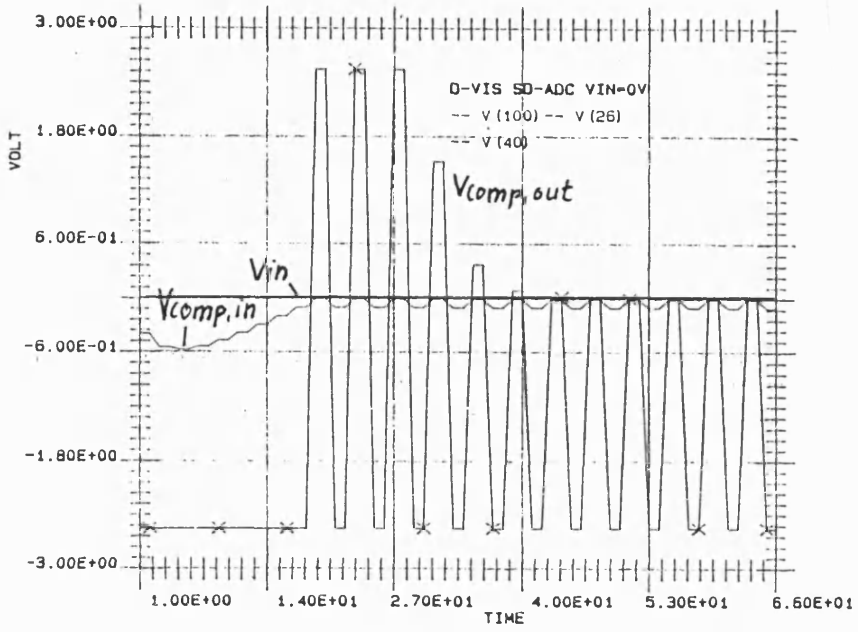

Figure 8.36 Vin = 0V

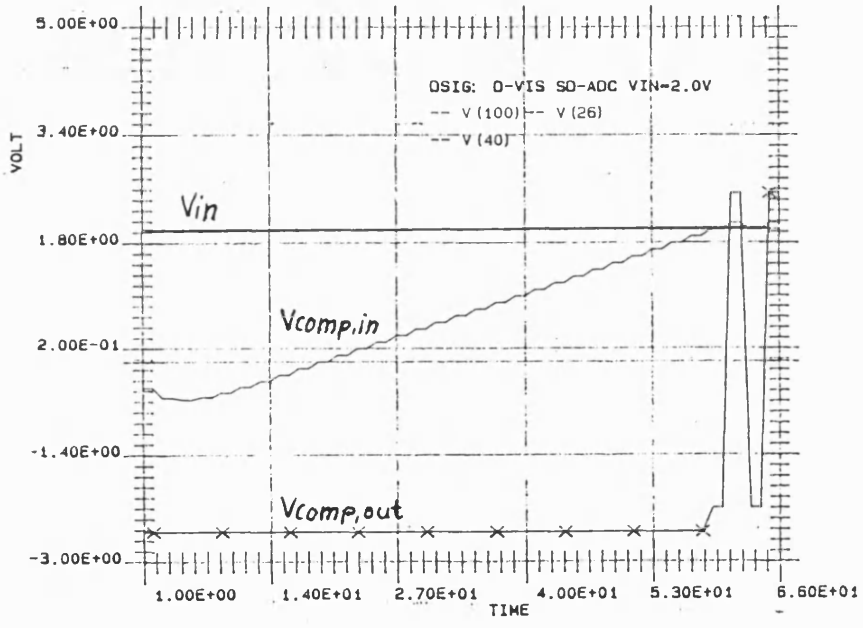

Figure 8.37 Vin = 2.0V

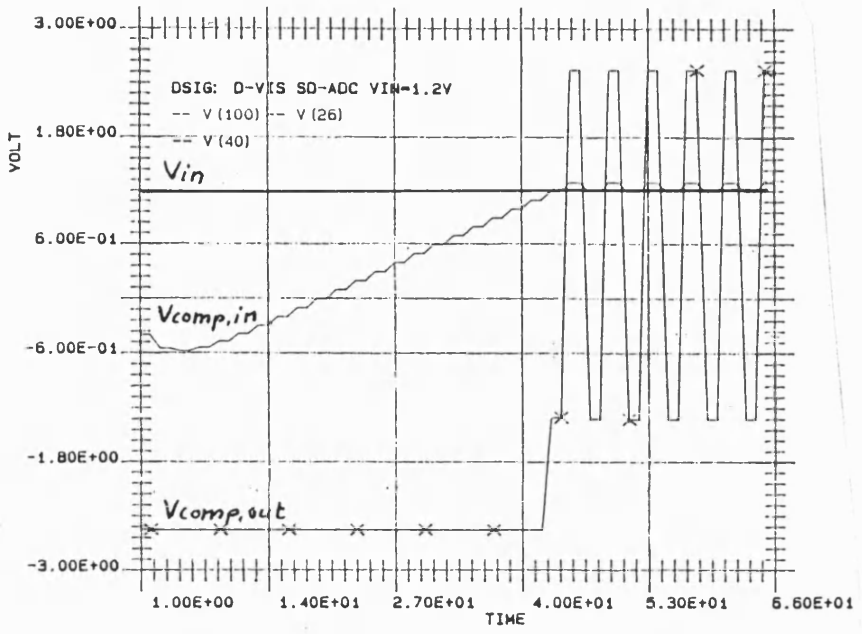

Figure 8.38 Vin = 1.2V

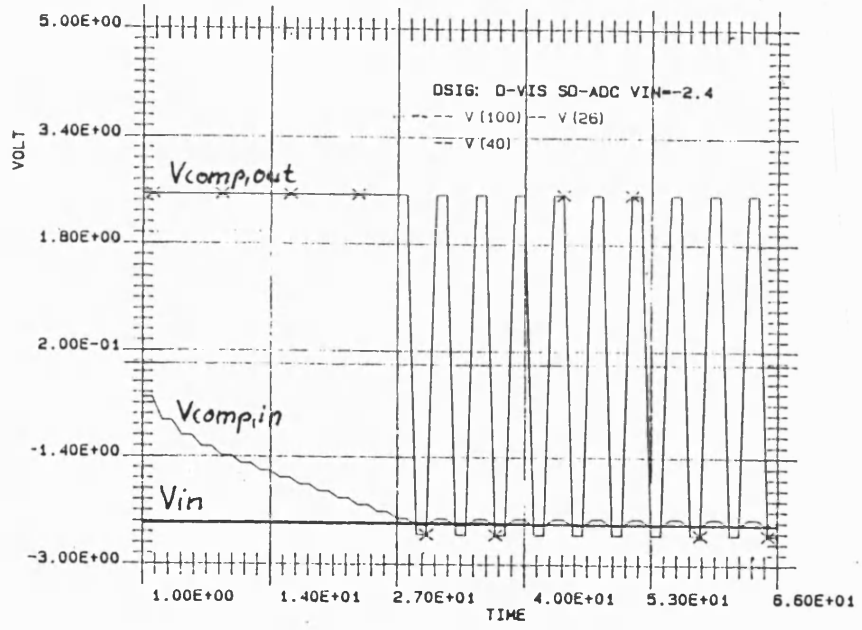

Figure 8.39 Vin = -2.4V

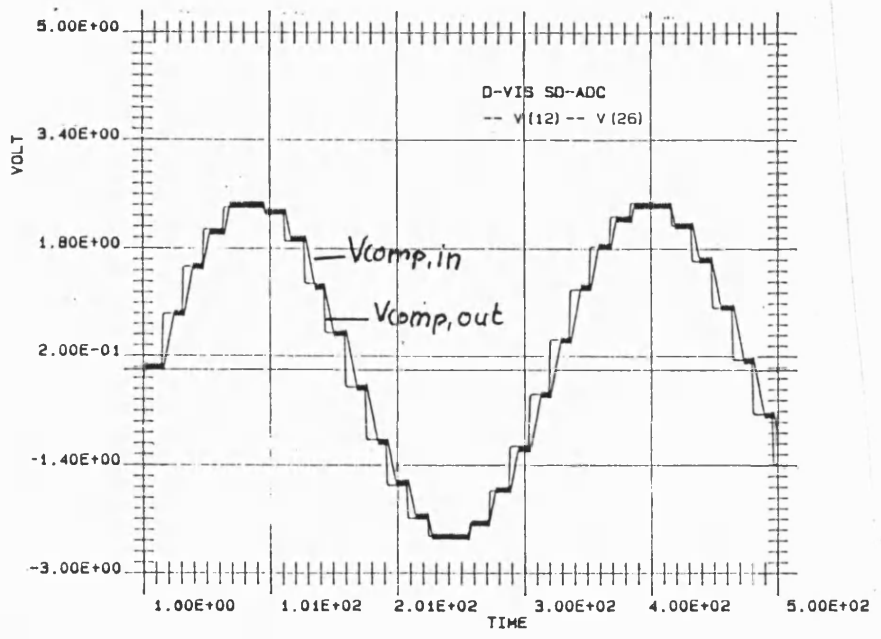

Figure 8.40 Vin = sine-wave with Fin = 594Hz Fsample = 1.67MHz

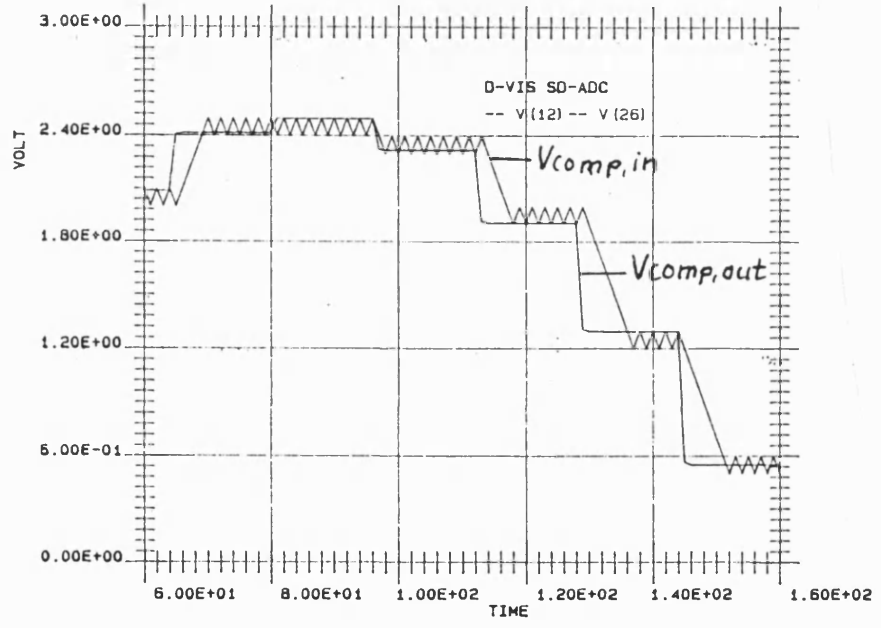

Figure 8.41 Zoom of figure 8.40

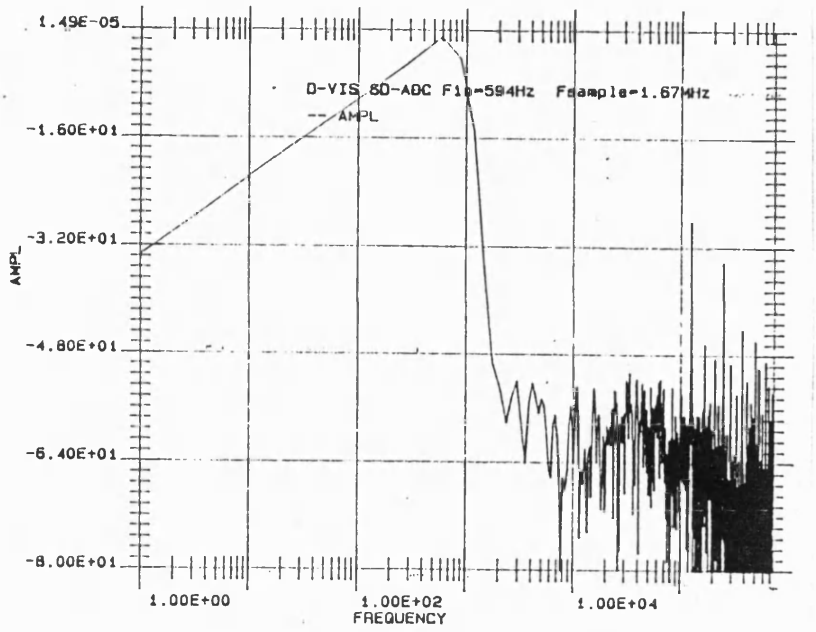

Figure 8.42 FFT result of the sine-wave in figure 8.40

The plots of figures 8.36 to 8.39 were created with an oversample factor of 512. This oversampling factor is a combination of the VIS cycles of 16 and the system oversample factor of 32. A different combination is shown in figures 8.40 and 8.41 over two sine-wave periods. The oversampling factor here is composed of VIS-cycles = 9 and the system oversampling factor is 16. The FFT result of figure 8.42 gives the signal to noise ratio of -72.6dB, that is the equivalent value for 12bit resolution.

8.8 Digital Control Unit and Digital Filtering

The switched capacitor circuits need a digital control unit. The principle to operate switched capacitor circuits is to have a non-overlapping clock system. In an integrated form this overlapping is made by a pair of inverter delay-chains and a NAND gate that combines both chains. To control the breadboard VIS-circuits, the digital control unit was built by using the circuits shown in figures 8.43 and 8.44.

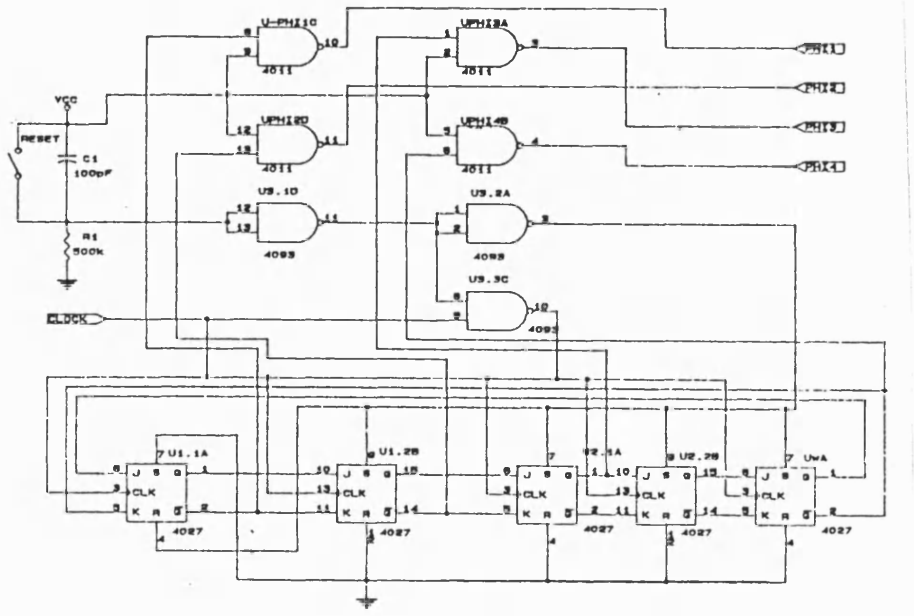

Figure 8.43 Clock Generator for VIS ADC Circuits

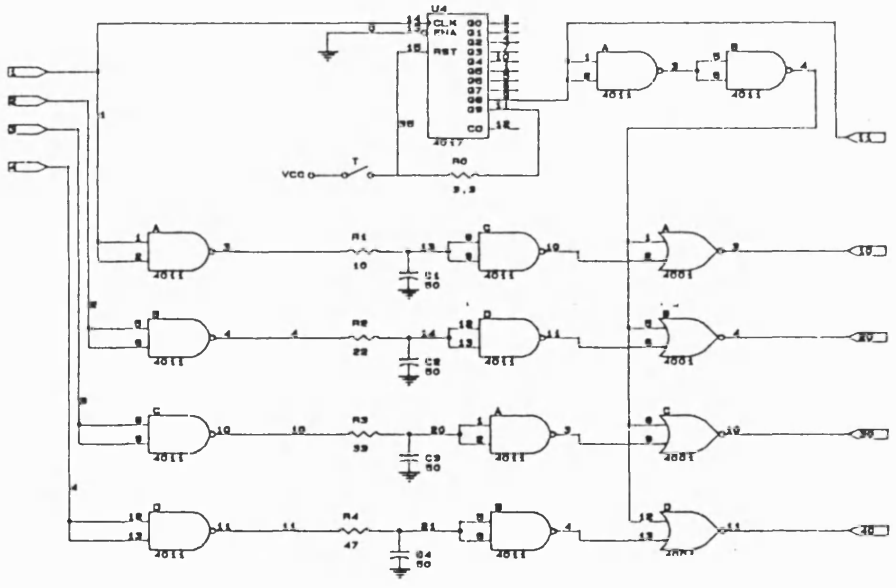

Figure 8.44 ADC - Clock Control Unit

The signal 0 is the "end of conversion (EOC)" signal, the signals PHI-1, PHI-2, PHI-3 and PHI-4 represent the clocks required for the internal ADC clock control.

The digital filtering used for the delta-sigma ADCs must be split into the decimation part and the low frequency low-pass filter. The decimation filter itself is

very simple, because of the use of a difference delta-sigma principle. This difference principle needs just an averaging, that means the digital output values of the comparator were averaged over one VIS cycle. This averaging decimates the high frequency sampling into a much lower frequency. Hence the oversampled staircase of the output can now be determined by the low-pass filter. This filter must be designed with regard to limit cycle sensitivity. The limit cycle sensitivity may be affected by multiplier overflow or by cutting after the multiplication. Therefore the limit cycle sensitivity is dependent on the structure of the digital filter. Because of the nature of passive filters, a digital filter derived from passive ones should be superior. The damping factor of limit cycles is very high in passive structures, because there is no energy to feed the filter. A digital filter structure that is derived from passive filter theory is the wave digital filter. Industrial applications show that the combination of wave digital filters with delta sigma ADCs seems very successful (e.g. SICOFI,a Siemens product).

8.9 Discussion

The discussion of the ADC will be split into discussion of the components and the discussion of the ADC principles.

8.9.1 Discussion of the Components

The first item to discuss is the advantage of operating with a switched capacitor design technique over a time continuous operation. Time continuous operation also needs clock control, the comparator needs a defined time point at which its output value is read. Also, correction terms used to balance the circuit need clock control. In time continous systems, all of these clocks are additional inputs to the signal path and result in a lot of distortion, e.g. jitter of the clocks. The time discrete operation of a

circuit results in a proper condition for all of the clocks and the charge-packages during each clock phase are exactly known.

The ADCs were simulated using the characteristics of the high-gain chopper OTAs. The high gain ensures that the error induced by the limitation of gain is kept as low as possible. In CMOS technologies, the gains of published operational amplifiers is about 80 to 90dB. This limitation is mostly based on the conductances of the transistors. Comparison with bipolar designs show that the conductances are much better, hence the gain of bipolar devices is bigger. But the current drawn is some orders of magnitudes bigger than CMOS devices. The other advantage of CMOS is that the charge flow into the capacitors can be discussed, because there is no constant input current needed to control the following stage. Using bipolar transistors requires a base-current to control the collector-emitter current. The chopper OTAs have a DC-gain of more than 110dB and therefore an accuracy of more than 18 bit. This enables these amplifier to be used for an accuracy of the ADC of 16 bit. The bandwidth is process dependent and was designed for worst-case (high temperature, low channel conductance and high threshold voltage) of about 20MHz. This value limits the sample rate of the ADCs, because of the settling time used for the desired accuracy.

The capacitors used for the charge splitting or charge conservation must be designed within their own well and must have an octagonal shape. This octagonal shape has the advantage that the etching process has least effect on the accuracy of the shape. Designing the capacitors with a ninety degree shape will often result in underetching effects and obviously this degrades the accuracy of the device. The capacitors belonging to a building block should be as close together as possible, to keep the effects of oxide thickness variations as low as possible.

Transfer-gates which are used in high accuracy designs should be designed with a guard ring, if possible. This is to avoid effects from the overshoot of the clocks,

which induces charges into the silicon. The guard ring absorbs most of these charges. Also the digital part is separated by a very low impedance guard ring connection from the analogue part. Both parts must have their own supply line.

8.9.2 Discussion of the new ADC Principles

The SA-ADC was introduced to show, that the Suàrez ADC [1] can be improved using VIS circuits to control the charge sharing during the SA-process. Suàrez achieved a resolution of 8bit in a conversion time of 100usec. Additionally he needed a DAC control to arrange the digital word as a direct function of the analogue input information. The SA-ADC presented in section 8.2 offers a resolution of 12 bit without a calibration cycle. No SA-register is needed to control the SA-process. This control is made with an EXOR logic. This EXOR compares the digital information of the actual and the delayed step. The A to D process is completed using an analogue memory cell. By including a calibration cycle the accuracy can be shifted towards 14 bit. More than 14 bit is not realistic, because of leakages in the analogue memory block. The conversion time is comparable to that published by Suàrez. The disadvantage of this ADC is the great number of building blocks.

The algorithmic ADC presented in section 8.3 offers 12 bit resolution without a calibration run and has 16 bit resolution by using a calibration cycle. This design requires a minimum number of components. The limit of accuracy is the matching property of the capacitors. This mismatch can induce a gain error in the factor-of-two amplifier or the difference between Vdd (Vdd/2) and the s&h input voltage is not accurate. These errors and the combination of these errors result in a constant shift of the ADC transfer curve. Therefore these errors can be regarded as a constant offset and can be calibrated by use of a digital calibration word.

Section 8.4 presents a one-stage delta sigma ADC. The difference between the DS-ADCs and those presented in the literature is the difference principle. This

difference principle is achieved by comparison with the input voltage and not as normal against signal ground. The advantage is the easy arrangement of the decimation filter, which is just an averaging filter. The average is taken as the digits per ADC step divided by the number of clocks during this cycle. The correction voltages are directly derived from the supply rails. Hence ringing of the supply lines affects the accuracy of this ADC.

The ADC of section 8.4 is now improved by including the VIS principle. The VIS circuit used herein is the I/V-VIS reference presented in chapter 5. The reference staircase is directed to the positive or negative input according to the decision of the comparator taken during the step before. The analogue value is stored in the integrator and is added with the appropriate reference voltage during the following step. The advantage of this procedure is that the correction values are the VIS reference voltages. Hence the accuracy of this procedure is increased in comparison to the previous method. Accuracies of 16 bit are achievable. The number of active elements is minimized. There is no digital control block required to operate these ADCs.

Additional improvements of the ADC principles shown above can be achieved by minimizing the influence of common mode signals due to clock feed through spikes and power supply ringing. Section 8.6 shows the results of the fully incremental VIS ADC. The incremental ADCs are very easy to read out. The result of the actual ADC step is added to, or subtracted from the result of the previous step depending on the comparator decision. The accuracy of this ADC is 16 bit. Theoretically, this accuracy is only limited by the finite gain of the amplifiers and the device matching. By using calibration procedures to calibrate the capacitances, for example with programmable trim capacitors, the accuracy can shifted to a maximum of 18 bit. The 18 bit accuracy is then limited by the amplifiers.

The next section shows the fully differential ADC as a delta sigma converter. The correction voltages are derived from the supply lines and are scaled by M=0.2 to achieve a proper balancing with the VIS reference staircase. The accuracy of this ADC

is 16 bit maximum.

As a conclusion of all the six different ADCs, the algorithmic principle and the incremental ADCs are best to use as analogue to digital interface building blocks. The delta sigma principle is not preferrable, because of the need for a digital filter circuit, which is a very critical element. Traditionally delta sigma ADCs were introduced in the art to achieve better resolutions by using standard building blocks. Recent publications show resolutions of 13 bit by using a special triple integration concept (MASH-principle [2]). Other delta sigma converters using two integrator stages offer about 12 to 13 bit accuracy. The standard ADC technique in CMOS technologies on the market is the McCreary array with a resolution of 8 to 10 bit. The principles presented during this work will change this situation. The accuracy can shift towards 14 to 16 bit range, if processes allow for small element tolerances.

REFERENCES CHAPTER 8

[1] Suaréz, Gray, Hodges "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques-Part II" IEEE, SC-10, Dec. 1975, pp. 379-385

[2] Matsuya Y., Uchimura K., Iwata A, Kobayashi T,. Ishikawa M., Yoshitome T., "A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping", IEEE Journal of solid-state circuits Vol.SC-22, No.6, pp.921-929, Dec.1987

CHAPTER 9

9. Conclusion

The object of this work was to create new A to D principles, to achieve a 16 bit range without the need of a trimming network. Achieving these results requires high accuracy in the different building blocks. New amplifier concepts based on the one stage OTA principle were presented. The technique used to improve the characteristics of the OTA circuit was the chopper technique, where the signal path remains time continous. A single ended chopper OTA with a unity gain frequency of 20 MHz and a DC-gain of more than 110dB and a fully differential OTA with a unity gain frequency of 15 MHz and a DC gain of more than 110dB were developed. These amplifiers shift the accuracy of the active element to more than 18 bits. The slew is fast enough to achieve maximum sample frequencies. The fully symmetric concept minimizes all the error voltages, that can be described as common mode signals, such as clock-feed through and ringing of the power supply lines. A new comparator design was presented that uses the fully symmetric technique paired with high speed operation characteristics. Based on a simple auto-zero inverter design, this comparator was built by two parallel auto-zero inverters, which are cross coupled from their outputs to the opposite inputs via a capacitor. This capacitor acts as a low impedance device at high frequencies, resulting in a high slew rate. The low-pass character means that the clock-feed through induced by the switches cannot influence the comparator function. The built in internal delay of this cross coupling results in a pre-reaction of each stage, before the high gain cross coupling process can be activated. At the end of the fast slew, the capacitor becomes more and more low impedance, so that the cross coupling effect is finished at the end of the comparison. The decision accuracy is better than 16 bit.

State of the art in industrial applications is the 8 bit Mc.Creary capacitor array ADC and the 12/13 bit delta sigma ADC. The 12 to 14 bit range can only be supported with the use of a calibration ADC technique. Herein, a DAC controls the last LSB accuracy by measuring the offset and by weighting the LSB correction charge. This process needs an additional DAC and a resistor string, to compute the correction values. Using the improved components, presented in Chapter 3, new building blocks for reference circuits and new A to D converters were developed. The most limiting factors to higher accuracy than about 14 bit is inaccurate charge splitting of capacitors, and the bigger tolerance mismatch by using resistor strings. A building block that measures the leakages before the charge splitting and offers the ability to add the measured and stored error voltage to the signal during the charge splitting process is the voltage inverter switch (VIS). Three different VIS circuits were researched and developed: the voltage follower VIS (V-VIS), the integrator VIS (I-VIS) and the fully differential VIS (D-VIS). It was found that the I-VIS and the D-VIS, which is based on the I-VIS principle, are the best circuits to achieve maximum accuracy in the charge charing. Using these circuits, VIS reference sources that produce a staircase up to a maximum resolution of 16 bit were presented in Chapter 5. The V-VIS and the I-VIS were built as breadboard test-devices. Thus simulation results could be verified with the measured results.

Analogue to digital converters based on the new components and using the VIS reference sources promise an improved accuracy. Chapter 7 presents six different A to D converter principles. In order to compare these an ADC that was published by Suàrez and which uses just a two capacitor array, an improved successive approximation A to D converter (SA-ADC) was initially developed. This SA-ADC has a VIS controlled charge distribution. The successive approximation control was minimized by introducing a self arranged SAR based on the exclusive OR function, that compares the digital output of the comparator between the current and the previous step. The

resolution was shifted from the 8 bit range presented by Suàrez towards 12 or 14 bit. 14 bit resolution is achievable if a calibration run every 1000 ADC cycles is included. The accuracy is limited to 14 bit because of the analogue memory cells.

The algorithmic principle is an A to D procedure that only uses the improved active components. There is no VIS control needed. The algorithmic procedure is a very simple principle, that needs no external digital control unit. The accuracy is 12 bit without calibration and 16 bit with a calibration run every 1000 A to D cycles. The upper passband is at 61.7KHz or 35.3 KHz with and without calibration respectively.

The other A to D principle is the incremental technique. This technique is a different arrangement of the resulting digital information, with a digital word added or subtracted in the digital register depending on the comparator decision. Therefore to operate an ADC with this technique, an incremental binary staircase is needed. This is the domain of the VIS reference circuit, which has an accuracy of 16 bit. Hence the incremental A to D converters need the improved active elements to achieve the maximum accuracy. Chapter 7 presents an incremental VIS-controlled sigma-delta ADC and a fully differential incremental VIS-controlled ADC. Both ADC's fulfil the high accuracy demand. The additional advantage of the fully differential concept is that the sensitivity to clock-feed through and ringing of the power supply lines is reduced.

Another principle, that is rearranged in this work is the delta-sigma (DS) principle. Traditionally the delta-sigma principle is used to achieve high accuracy 12- to 13-bit without the use of the much more complicated calibration ADCs. This principle requires a decimation filter and afterwards a digital low-pass filter. The main idea is to use the integrator as a noise shaping component in order to minimize the noise in the baseband. The DS principle was slightly changed: the reference voltage of

the comparator is not the signal ground, as usual. The input voltage is also used as the reference voltage of the comparator. This technique offers a very simple decimation technique that can be regarded as an averaging filter. The digital values of the comparator are averaged by the number of VIS cycles used for one ADC step. With this technique, a standard Candy DS-ADC was developed. DS-ADCs using the incremental and fully differential incremental principle were additionally developed and simulated. All of these A to D principles offer up to the 16 bit range. In contrast to standard oversampled devices, the oversampling factor is split into the factor used for the internal VIS staircase -normally 16- and the system oversampled factor that should normally be arranged by an n^2 number.

Simulations of these A to D converters were done using BONSAI and the SC-program. BONSAI has had a lot of problems in simulating the highly sophisticated A to D processes. Long simulation times and an increased number of iteration errors forces the development of a simulator for switched capacitor circuits that can be digital controlled. The SC-program offers the ability to simulate switched capacitor building blocks including some digital components, delays, summation blocks and multipliers. The SC-program was compared against the results achieved with BONSAI and showed a perfect agreement. Hence all of the A to D converters could be simulated with a large number of steps.

Further work in the field of new A to D converter should research the combination of the VIS controlled charge sharing with the summation of the integrator. This would combine the VIS staircase reference with the sigma used to arrange the incremental steps. The limitations of the bandwidth are obviously dependent on the unity gain bandwidth of the amplifier and therefore a limitation forced by the process. Improvements may be achieved by using other technologies, e.g. gallium-arsenide. The noise behaviour of the new delta-sigma ADCs should be

researched and two-stage or triple-integrator (MASH) DS-ADCs might open the way for more than 16 bit accuracy. The basic idea of the DS-principle is to achieve higher accuracy with the help of the statistical distribution of the digital data train and the noise shaping characteristic of an integrator. The integrator need not be an analogue integrator. The integration process can also be shifted to the digital side. The next item to discuss is the digital filter. As discussed in Chapter 8, the wave digital filter will offer a design that is very stable against limit cycle sensitivity. The wave digital filter proposed for the high resolution ADC is a bridge filter, because bridge filters have maximum symmetry. Therefore oscillations of the limit cycle that might occur are cancelled at the output section of the filter, in which both bridge branches are added. The limit cycles that might occur have a high probability of being equivalent, as the branches are exactly mirrored.

APPENDIX I

The C-V Curve

There are innumerable publications on the behaviour of silicon - silicon dioxide systems. The most relevant ones are [AI.1] to [AI.10]. A summary of equations to calculate the C-V behaviour is given below.

basic equations

$$V_T = \frac{k \cdot T}{e} \qquad (AI.1)$$

$$L_{DB} = \sqrt{\frac{\varepsilon_{Si} \cdot \varepsilon_0 \cdot V_T}{e \cdot n_i}} \qquad (AI.2)$$

$$V_B = \ln\left(\frac{N}{n_i}\right) \qquad (AI.3)$$

V_T is the temperature voltage

L_{DB} is the Debye length

V_B is the bulk Fermi potential coefficient

V_B is positive for p-type material and is negative for n-type material

N is the concentration of the majority charge carriers in doped silicon zones. N can be either N_A for the acceptor concentration by using p-type material and N_D for the donor concentration by using n-type material.

n_i is the free electron concentration in intrinsic silicon.

$$Q_K = \frac{\varepsilon_0 \cdot \varepsilon_{Si} \cdot V_T}{L_{DB}}$$

$$Q_B = -2 \cdot \sqrt{\varepsilon_0 \cdot \varepsilon_{Si} \cdot e \cdot N \cdot V_T \cdot |V_B|} \qquad (AI.4)$$

Q_K is the charge coefficient

Q_B is the space charge per unit area

Calculation of the minimum capacitance for high frequencies

$$C_{HF,\min} = \frac{\varepsilon_0 \cdot \varepsilon_{Si}}{L_{DB}} \cdot \sqrt{\frac{N}{8n_i \cdot V_B}} \qquad (AI.5)$$

Calculation of the minimum capacitance for low frequencies

$$C_{LF,\min} = \frac{\varepsilon_0 \cdot \varepsilon_{Si}}{L_{DB}} \cdot \sqrt{\frac{N}{2n_i}} \cdot \frac{1}{1 + 0.542 \cdot V_B - 0.0115 \cdot V_B^2 - 1.25 \cdot 10^{-4} \cdot V_B^3} \qquad (AI.6)$$

Calculation of the flat band capacitance

$$C_{FB} = \frac{\varepsilon_0 \varepsilon_{Si}}{L_{DB}} \cdot \sqrt{\frac{N}{2 \cdot n_i}} \qquad (AI.7)$$

Calculation of the differences of the work functions

$$\Phi_{MS} = \Phi_M - \left(\Phi_{SO} - \frac{E_G}{2} - \Phi_F \right) \qquad (AI.8)$$

Φ_{MS} is the metal to silicon work function

Φ_{M} is the metal to oxide work function

Φ_{SO} is the semiconductor to oxide work function

Φ_{F} is the bulk Fermi potential

E_G is the semiconductor band gap voltage

Calculation of the threshold voltage

$$V_{TH} = V_{FB} + 2 \cdot (E_F - E_i) + \frac{Q_B}{C_{ox}} V \qquad (AI.9)$$

V_{TH} is the threshold voltage

Calculation of the surface potential coefficient

$$V_S = V_{HL} \cdot \frac{e}{kT} - V_B \qquad (AI.10)$$

V_{HL} is the contact potential of the semiconductor

Calculation of the MIS potential

$$V = V_{HL} - \frac{\varepsilon_0 \cdot \varepsilon_{Si} V_T}{L_{DB} \cdot C_{Ox}} \cdot F(V_S, V_B) \qquad (AI.11)$$

The term $F(V_S,V_B)$ will be explained later in the appendix.

Calculation of the low frequency capacitance of the MOS structure

$$C_{LF} = -\frac{\varepsilon_0 \cdot \varepsilon_{Si}}{L_{DB}} \cdot \left(\frac{\sinh V_S - \sinh V_B}{F(V_S, V_B)} \right) \qquad (AI.12)$$

if $V_S = V_B$:

$$C_{LF} = \frac{\varepsilon_0 \cdot \varepsilon_{Si}}{L_{DB}} \cdot \sqrt{\cosh V_B} \qquad (AI.13)$$

The capacitances within a C-V characteristic will be normalised to the oxide capacitance from the accumulation mode.

$$C_{Ox} = \frac{\varepsilon_0 \cdot \varepsilon_{Ox}}{t_{Ox}} \qquad (AI.14)$$

The space charge function $F(V_S, V_B)$ is dependent on the density of space charges derived by Poisson's law, which defines the density of the space charges within silicon.

The concentration of free carriers is given by:

$$n = n_i \cdot e^{V/V_T}$$

for minority charge carriers and

$$p = p_i \cdot e^{-V/V_T}$$

for majority charge carriers.

where:

V is the potential difference between flatband condition and the intrinsic Fermi potential level. u is 0 in the bulk of the semiconductor and is defined as the surface potential u_s at the Si-SiO_2 interface.

n_i, p_i are the intrinsic charge carrier concentration of n- and p-diffusion

The computation of the density of the space charges can now be done with Poisson's law defined for the potentials for the space charges:

$$\frac{\partial^2 V}{\partial x^2}+\frac{\partial^2 V}{\partial y^2}+\frac{\partial^2 V}{\partial z^2}=-\frac{\rho(x,y,z)}{\varepsilon_{Si}} \qquad (AI.15)$$

where: $\rho(x,y,z)$ is the density of the space charges.

Solving eqn (AI.15) can be simplified by considering one dimensional space. Hence the density of the space charges can be written as:

$$\rho(x) = x_q \cdot (N_D - N_A) \qquad (AI.16)$$

$$N_D - N_A = n_i \cdot e^{V/V_T} + n_i \cdot e^{-V/V_T} \qquad (AI.17)$$

$$N_D - N_A = 2 \cdot n_i \cdot \sinh\frac{V}{V_T} = 2 \cdot n_i \cdot \sinh\frac{\Phi_F}{V_T} \qquad (AI.18)$$

Using eqn. (AI.18), eqn (AI.15) can be simplified by:

$$\frac{\partial^2 \Phi}{\partial x^2} = -\frac{2 \cdot e \cdot n_i}{K \cdot \varepsilon_0 \cdot \varepsilon_{Si}} \cdot \left(\sinh \frac{\Phi_F}{V_T} - \sinh \frac{\Phi_S}{V_T} \right)$$

$$\frac{\partial^2 V}{\partial x^2} = -\frac{2 \cdot e \cdot n_i}{K \cdot \varepsilon_0 \cdot \varepsilon_{Si}} \cdot (\sinh V_B - \sinh V_S) \qquad (AI.19)$$

where:

Φ_F is the bulk Fermi potential.

Φ_S is the silicon surface potential.

V_S is the surface potential coefficient

$$L_{DB} = \sqrt{\frac{\varepsilon_0 \cdot \varepsilon_{Si} \cdot V_T}{e \cdot n_i}}$$

$$\frac{\partial^2 V}{\partial x^2} = \frac{\sinh V_S - \sinh V_B}{L_{DB}^2} \qquad (AI.20)$$

Integration of eqn (AI.20) gives the electrical field intensity caused by the space charge potential. Rearrangement of this electrical field results in the electrical field coefficient or the space charge coefficient $F(V_S, V_B)$.

$$\int_0^{\frac{\partial V}{\partial x}} \frac{\partial}{\partial x} \cdot d\left(\frac{\partial V}{\partial x} \right) = \frac{1}{L_{DB}^2} \cdot \int_{V_B}^{V} (\sinh V_S - \sinh V_B) dV \qquad (AI.21)$$

$$\frac{\partial V}{\partial x} = \pm \sqrt{\frac{2}{L_{DB}}} \cdot \sqrt{(V_B - V_S) \cdot \sinh V_B - \cosh V_B + \cosh V_S} \qquad (AI.22)$$

$$\overline{E} = -\frac{\partial V}{\partial x} = \pm \frac{V_T}{L_{DB}} \cdot F(V_S, V_B) \qquad (AI.23)$$

$$F(V_S, V_B) = sign(V_B - V_S) \cdot \sqrt{2 \cdot ((\cosh V_S - \cosh V_B) + (V_B - V_S) \cdot \sinh V_B)} \qquad (AI.24)$$

The space chage per unit area versus the surface potential gives information about accumulation, weak inversion and strong inversion. The space charge is defined by the electrical field intensity induced by the surface charges:

$$Q_S = -\varepsilon_S \cdot \overline{E}_S$$

$$Q_S = \pm \frac{\sqrt{2} \cdot V_T}{L_{DB}} \cdot F(V_S, V_B) \qquad (AI.25)$$

The equations shown above were used in a program to generate theoretical CV-characteristics in order to predict the internal silicon potentials, the band characteristics and the low/high frequency behaviours of the silicon varactor effect [AI.11]. Table AI.1 shows the first part of the ASCII output file, giving all the static information. Figures AI.2 and AI.3 show the C/COX characteristic against the MIS voltage and the space charge per unit area against the surface potential, respectively. Figure AI.3 gives information about the different operating regions of a semiconductor. The QS characteristic of the negative surface potential represents the accumulation region, positive values of the surface potential force the MIS structure to operate in the inversion range. Beyond the QS-pole, within the positive surface potential range, the MIS structure is inverted. The weak inversion range spans up to a surface potential of about 0.7V. This region is characterized by a nearly constant range of the QS-curve.

The significant increase of the QS characteristic at about 0.7V surface potential shows the point at which the strong inversion range begins. Figure AI.4 shows a detailed plot in which all the work functions and potentials used within this section are explained.

CV - CURVE (Vers. 1.0 W.Tenten Gammertingen 01.10.1988) Testfile: TEST2 Date : 5.10.1988

The test temperature is	:	20.000	Grd. Cels.
The probe is P-type silicon with	:		
Thickness of the OXIDE	:	175.00	nm
Permittivity of the OXIDE	:	3.8400	
Capacitance of the OXIDE	:	146.77	pF
Density of free majorities	:	.22000E+16 1/cm**3	
Majority concentration in intrinsic silicon	:	.76100E+10 1/cm**3	
Debye length	:	.32810E-02 cm	
Charge coefficient	:	.79900E-11 AS/cm**2	
Relative capacitance minimum of			
- HF-curve	:	.46558	
- LF-curve	:	.49730	
Relative capac. of flat band	:	.86070	
Metal to oxide work function	:	3.0000	V
Semic. to oxide work function	:	3.2500	V
Metal to silicon work function	:	.62054	V
Flat band voltage	:	-.21015	V

Fermi-Potential of bulk material	:	-.31804 V
Space charge per unit area	:	-.21544E-07 AS/um**2
Threshold voltage	:	-.62038 V

Table AI.1 CV static characteristics produced by the programme "CVC"

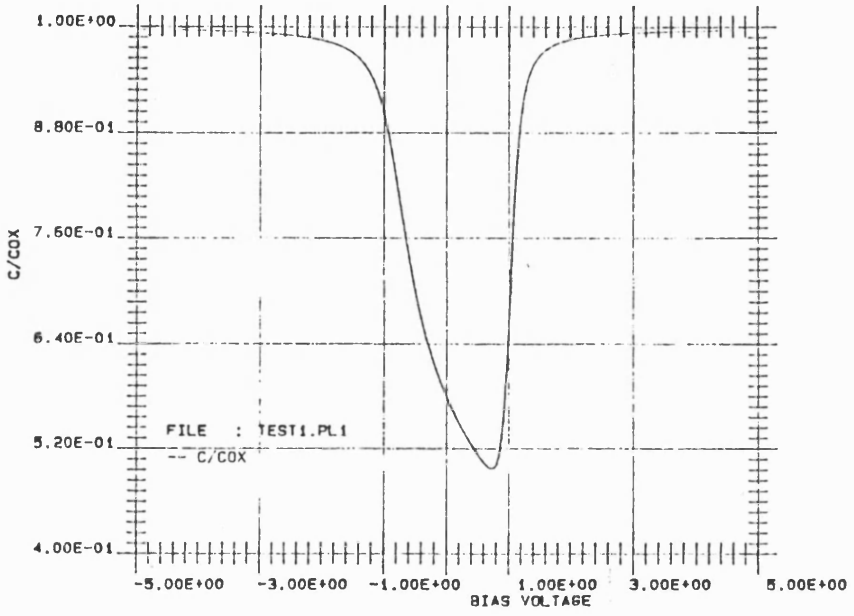

Figure AI.2 C/Cox = f(V) characteristic

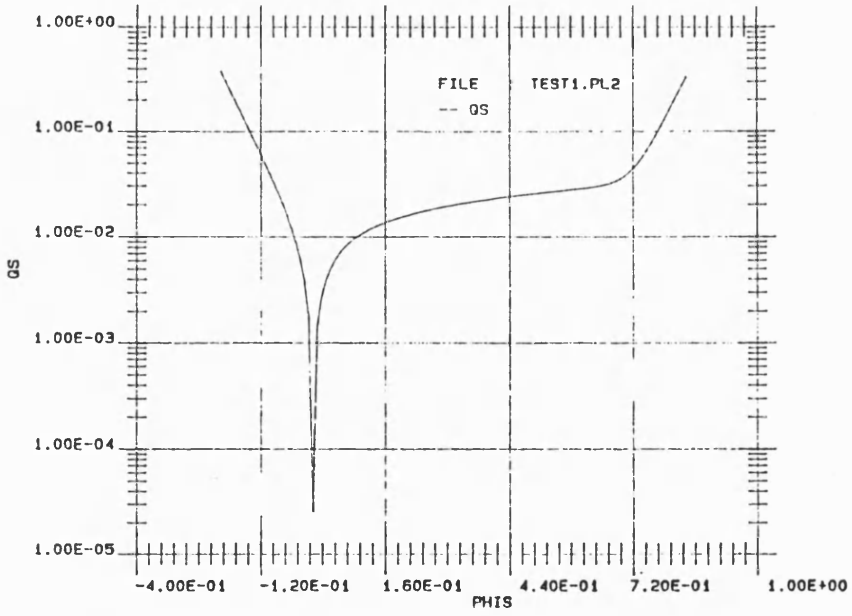

Figure AI.3 QS = f(PHIS) characteristic

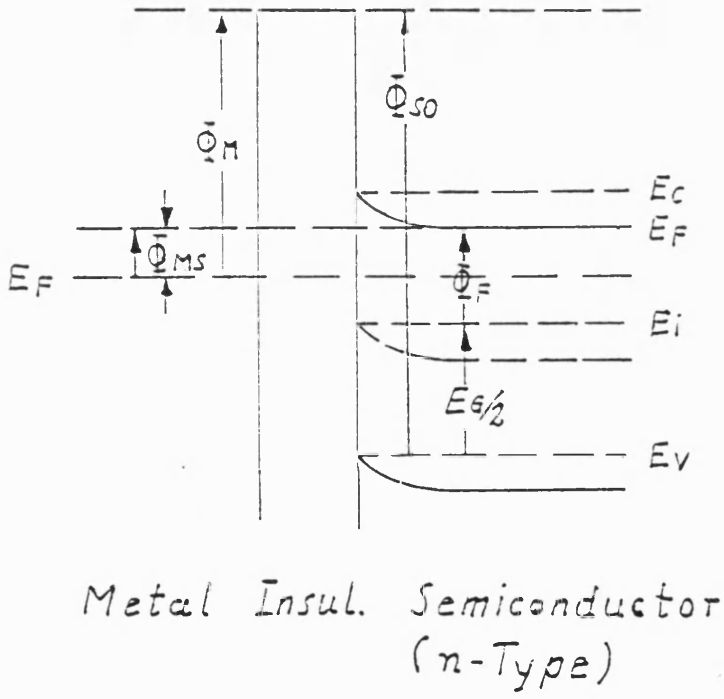

Figure AI.4 Work functions and potentials in a MIS structure

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[AI.7] Kingston R.H., Neustadter S.F., "Calculation of the space charge, electric field, and free carrier concentration at the surface of a semiconductor", Journal of applied physics 26, pp. 718 - 720, 1955

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[AI.10] Brews J.R., "A comparison of MOS inversion layer charge and capacitance formulas", IEEE Transactions on Electron Devices, ed. 33, No.2, pp. 182 - 187, Feb. 1986

[AI.11] Tenten, W. "CVC, a programme to compute the CV-characteristics of silicon", V1.0, Gammertingen W.Germany, 1.10.1988

APPENDIX II

Theoretical Approach to the Fringing Correction Terms

Figure II.1 shows a cross section of an interconnect line over silicon.

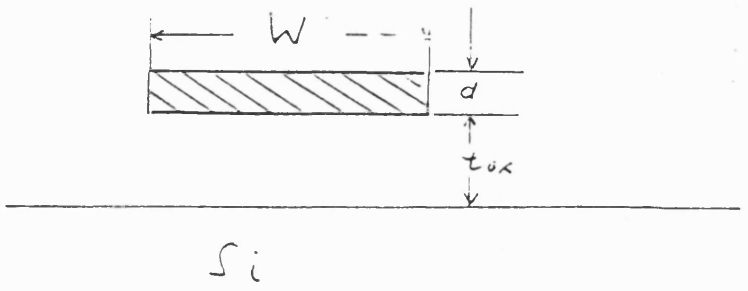

Figure II.1.

A current flowing through the interconnect line produces an electrical and a magnetic field.

The resulting Pointing vector is

$$\vec{S} = \vec{E} \cdot x \cdot \vec{H} \qquad (II.1)$$

if: $t_{ox}, W < \frac{\lambda}{2}$

where λ is the wave length

Any discussion of electromagnetic waves needs an auxiliary circuit of an interconnect line.

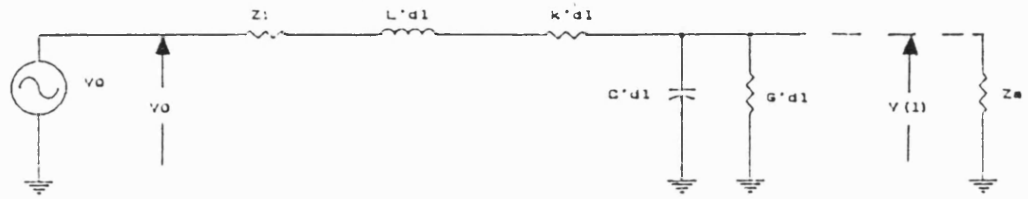

Figure II.2. Interconnect Line Auxiliary Circuit

The overall impedance is given by

$$z = \sqrt{\frac{k' + j\omega L'}{G' + j\omega C'}} \qquad (II.2)$$

where

L' is the geometry dependent inductance

C' is the geometry dependent capacitance

If ohmic losses can be neglected eqn (II.2) is approximated by:

$$z \approx \sqrt{\frac{L'}{C'}} \qquad (II.3)$$

We also have

$$\gamma = \alpha + j\beta \qquad (II.4)$$

where

γ is the propagation constant

α is the damping constant

$j\beta$ is the phase constant

$$\alpha = \sqrt{k'C' - \omega^2 C'L'}$$

$$j\beta = \sqrt{j\omega C' \cdot (L' + k')}$$

The electric field component is given by:

$$Q = \oint D dA$$

$$V = \int E ds \qquad (II.5)$$

$$C = \frac{Q}{V}$$

where

Q is the induced electric charge

$\overline{D} = \varepsilon_0 \cdot \varepsilon_r$ $\overline{E}$ *is the electrical displacement*

A is the cross sectional area of the interconnect line

The magnetic field component is given by:

$$I = \oint jdA = \oint Hds \qquad (II.6)$$

$$\Phi = \oint BdA$$

$$L = \frac{\Phi}{I}$$

where:

$\overline{B} = \mu \cdot \overline{H}$

μ is the magnetic permeability constant

$\mu = \mu_1 \cdot \mu_0$

$\mu_0 \approx 4 \cdot \pi \cdot 10^{-11} \cdot \frac{Vs}{Am}$

I is the magnetically induced current

Φ is the magnetic flux

L is the inductance

The charge flow into a capacitance is given by:

$$Q = \oint DdA = \varepsilon \quad |E| \cdot A = \varepsilon \quad |E| \cdot W \cdot L \qquad (II.7)$$

The capacitance per unit area can be written by using eqn. (II.7):

$$C = \frac{Q}{V} \cdot \frac{1}{L} = \frac{\varepsilon \ |E| \cdot W \cdot L}{|E| \cdot t_{ox} \cdot L} = \varepsilon \cdot \frac{W}{t_{ox}} \qquad (II.8)$$

The inductance of the interconnect line can be expressed as:

$$L' = \frac{\Phi'}{I} = \frac{\mu \cdot |H| \cdot t_{ox}}{|H| \cdot W} = \mu \cdot \frac{t_{ox}}{W} \qquad (II.9)$$

The wave resistance is given by:

$$z = \sqrt{\frac{L'}{C'}} = z_0 \cdot \sqrt{\frac{\mu}{\varepsilon}} \cdot \frac{t_{ox}}{W} \qquad (II.10)$$

If

$d << t_{ox}$

$W << L$

eqn. (II.8) to (II.10) can be simplified using:

$$\int_0^d \frac{1}{x} dx \approx \ln \frac{4t_{ox}}{d} \qquad (II.11)$$

$$\int_0^{W/2} \frac{1}{x} dx \approx \ln \frac{4t_{ox}}{W/2} \qquad (II.12)$$

Hence the following equations describe the approximate capacitance, inductance and impedance of the interconnect line:

$$C' = \frac{2 \cdot \pi \cdot \varepsilon}{\ln \frac{8t_{ox}}{W}} \qquad (II.13)$$

$$L' = \frac{\mu}{2\pi} \cdot \ln \frac{8t_{ox}}{W} \qquad (II.14)$$

$$z = \sqrt{\frac{L'}{C'}} = \frac{z_0}{2\pi} \cdot \sqrt{\frac{\mu}{\varepsilon}} \cdot \ln \frac{8t_{ox}}{W} \qquad (II.15)$$

Following Wheeler [AII.1]the correction term for the capacitance of an interconnect line can be written with and without the thickness of the interconnect line:

$$k = 1 + \frac{1}{W/t_{ox}} \cdot \left(2.42 - 0.44 \cdot \frac{1}{W/t_{ox}} + \left(1 - \frac{1}{W/t_{ox}} \right)^6 \right) \qquad (II.16)$$

$$k = 1 + \frac{1}{W/t_{ox}} \cdot \left(2\frac{\pi}{T} \right) \qquad (II.17)$$

where:

$$T = \ln \left(1 + 2\frac{t_{ox}}{d} + \sqrt{\frac{2t_{ox}}{d} \cdot \left(2\frac{t_{ox}}{d} + 2 \right)} - \frac{1}{2\frac{t_{ox}}{d}} \right)$$

$$C = C' \cdot k$$

[AII.1] Wheeler H.A., "Transmission-line properties of parallel strips separated by a dielectric sheet", IEEE Transactions on Microwave Theory and Techniques", pp. 172 - 185, March 1965

APPENDIX III

Integration Procedures Applied in Spice and BONSAI Numerical Integration Methods

In common use in simulation software are the following numerical integration procedures:

1.) forward Euler

2.) backward Euler

3.) trapezoidal or implicit

4.) Gear

Bonsai uses the trapezoidal method because of its stability range that is the whole negative half plane of real numbers. Spice mostly use the Gear method. It will be shown, that the Gear methods are critical in certain applications because of their stability range.

III.1 Forward and Backward Euler

Based on the differential equation

$$\frac{dx}{dt} = \lambda \cdot x \qquad (III.1)$$

the exact solution is:

$$x = x_0 \cdot e^{\lambda t}$$

$$x_0 = x(t = 0) \qquad (III.2)$$

The forward Euler procedure uses:

$$x_{n+1} = x_n + h \cdot \lambda \cdot x_n = x_n \cdot (1 + h \cdot \lambda)$$

$$x_n = x_0 \cdot (1 + h \cdot \lambda)^n$$

$$x_n = x \cdot (t = n \cdot h) \qquad (III.3)$$

where: h is the step width

The system is stable if

$$| 1 + h \cdot \lambda | =< 1 \qquad (III.4)$$

The backward Euler uses:

$$X_{n+1} = x_n + h \cdot \lambda \cdot x_{n+1} = x_n \cdot \frac{1}{1 - h \cdot \lambda} \qquad (III.5)$$

$$x_n = x_0 \cdot \left(\frac{1}{1 - h \cdot \lambda} \right)^n$$

The system is stable if:

$$| 1 - h \cdot \lambda | \geq 1$$

It is to be noted that the smallest time constant sets the step width.

III.2 Trapezoidal - Integration

(Implicit of 2nd order)

The differential equation

$$x_{n+1} = x_n + h \cdot \frac{dx_n}{dt} + \frac{h^2}{2} \cdot \frac{d^2x_n}{dt^2} \qquad (III.6)$$

will be solved. The equation system can be arranged as:

$$\frac{dx_{n+1}}{dt} = \frac{dx_n}{dt} + h \cdot \frac{d^2x_n}{dt^2}$$

$$\frac{d^2x_n}{dt^2} = \frac{1}{h} \cdot \left(\frac{dx_{n+1}}{dt} - \frac{dx_n}{dt} \right) \qquad (III.7)$$

$$x_{n+1} = x_n + \frac{h}{2} \cdot \left(\frac{dx_n}{dt} + \frac{dx_{n+1}}{dt} \right)$$

with $dx/dt = \lambda \cdot x$, consideration of the stability range gives:

$$x_{n+1} = x_n + \frac{h \cdot \lambda}{2} \cdot (x_n + x_{n+1})$$

$$x_{n+1} = x_n \cdot \frac{1 + \frac{h \cdot \lambda}{2}}{1 - \frac{h \cdot \lambda}{2}} = x_n \cdot \rho \qquad (III.8)$$

where

ρ is the recursion or reproduction factor

The system is stable if:

$$\left| \frac{1 + \frac{h \cdot \lambda}{2}}{1 - \frac{h \cdot \lambda}{2}} \right| \leq 1 \qquad (III.9)$$

Hence the real number of $h \cdot \lambda$ must be in the negative half plane.

III.3 Gear Method

The Gear differential equation can be written as

$$\frac{dx_{n+1}}{dt} = \sum_{i=0}^{k} \alpha_i \cdot x_{n+1-i} \qquad (III.10)$$

The eqn.(III.10) can be arranged by its interpolation polynominal system of order k as:

$$x(t) = a_0 + a\,1(t_{n+1} - t) + \ldots + a_k(t_{n+1} - t)^k$$

$$\begin{bmatrix} x_{n+1} \\ x_n \\ x_{n-1} \\ \cdots \\ \cdots \\ \cdots \\ x_{n+1-k} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \\ 1 & h & h^2 & \cdots & h^k \\ 1 & 2h & (2h)^2 & \cdots & (2h)^k \\ . & . & . & \cdots & . \\ . & . & . & \cdots & . \\ . & . & . & \cdots & . \\ 1 & kh & (hk)^2 & \cdots & (hk)^k \end{bmatrix} * \begin{bmatrix} a_0 \\ a_1 \\ a^2 \\ . \\ . \\ . \\ a^k \end{bmatrix}$$

where:

$$-a_1 = \alpha_0 \cdot a_0$$

$$+\alpha_1(a_0 + ha_1 + \ldots. + h^k \cdot \alpha_k)$$

$$+\alpha_2(a_0 + 2ha_1 \ldots. + (2h)^k \cdot a_k)$$

$$+$$

.

.

.

$$+\alpha_k(a_0 + kha_1 \ldots. + (kh)^k \cdot a_k) \qquad (III.12)$$

Comparison of coefficients give the matrix:

$$\begin{bmatrix} 0 \\ -1 \\ 0 \\ . \\ . \\ . \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & \dots & 0 \\ 0 & h & 2h & \dots & kh \\ 1 & h^2 & (2h)^2 & \dots & (kh)^k \\ . & . & . & \dots & . \\ . & . & . & \dots & . \\ . & . & . & \dots & . \\ 0 & h^k & (2h)^k & \dots & (kh)^k \end{bmatrix} * \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ . \\ . \\ . \\ a_k \end{bmatrix}$$

k = 1 gives the Gear of first order.

$$\alpha_0 + \alpha_1 = 0$$

$$\alpha_1 \cdot h = -1$$

$$\alpha_1 = -\frac{1}{h}$$

$$\alpha_0 = \frac{1}{h}$$

$$\frac{d_{xn+1}}{dt} = \frac{1}{h} \cdot (x_{n+1} - x_n) \qquad (III.14)$$

Eqn. (III.14) is identical to the backward Euler equation (III.5). Figure III.1 shows the regions of stability of the gear-methods up to K=6, where "S" signs the stability plane and "US" signs the unstable plane.

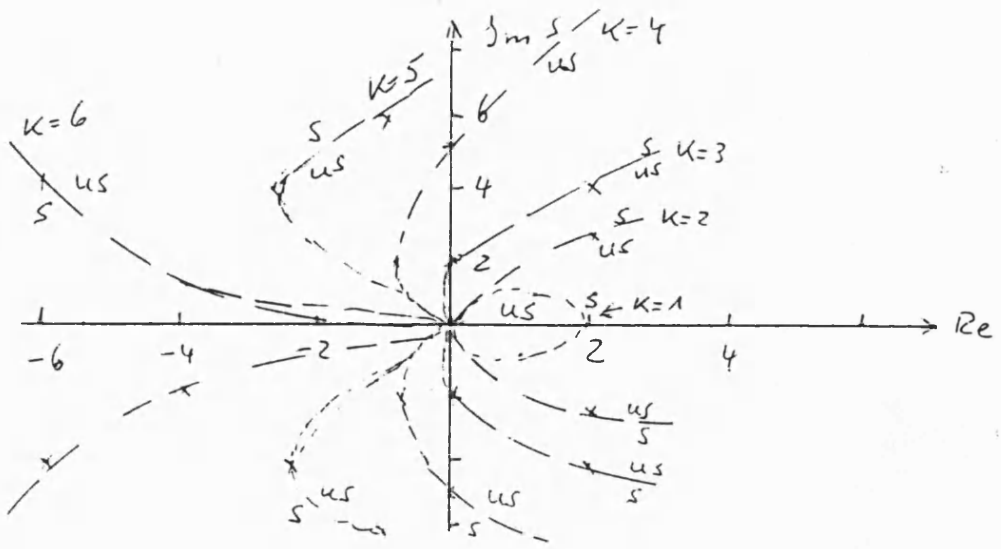

Figure III.1 Stability regions of the GEAR-integration method

Because of the nonlinear characteristic of the stabilty ranges, this integration method is critical to use, by exceeding the order of 2.

APPENDIX IV

S C - M A N U A L

VERSION 2.3

(03.05.1989)

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Welcome to the SC-program. This program fills a gap between network simulation tool like BONSAI, SPICE etc. and switched capacitor (SC) simulators like DOSCA, SWITCAP etc.

The computer power required to run this program is:

IBM AT or compatible with 640K RAM and a math coprocessor 80287.

This program belongs to a program line that also contains:

TPLOT: A plot program incorporating special options like zooming, arithmetic operations, HPGL interface and linear regression.

MURF: A Multiradix FFT program including 13 different windows, data selection of the time domain data train, sinx/x correction and distortion analysis.

1. Introduction

The SC-simulator computes actual nodal voltages in the time domain based on the transfer function of library elements. There are 21 library elements built into the program. There are three different types of voltages, i.e. linear or triangular shape, constant or square shape and sinusoidal shape. These cards enable the user to create up to 50 different voltage sources as clocks or input voltages. To use these elements nodals must be defined by nodal numbers; capacitances, gain factors and so forth by

their specified values. The next section describes library element definition. The program structure itself is split by command words, defined with a dot "." in front. Between these command words, the user can create a file without any restriction.

2. File - Conventions

The program needs no formatted input. Hence the structure of the input file that defines the circuit to be simulated depends on the user. There is only one limit: the maximum line width is set to 80 characters per line. There are two output files produced by the program:

filename.SOU
filename:SPL

where the .SOU file shows the input declarations and the simulated results in ASCII format, and the .SPL file is a binary file, which can be used with the TPLOT and MURF program. The input file can be arranged using capital or small letters. Structured files are also allowed. Up to 5 blank lines are valid. Comments must begin with a $ label.

The + sign at the beginning of each line signifies an additional line for the last element declarator. One exeption: There is no need for the + sign within the .INIT declarations.

3. DOT Syntax Description

The program is split by dot cards. Using the dot cards forces the program to manage the input checks, the simulation runs and the printing of the files.

.TITLE Using this card, up to three title lines may be defined. These title lines are helpful to identify the simulation runs. The title lines will be repeated at the beginning of each new print cluster. A print cluster is a print block consisting of the input section and the output section. It is automatically split if more than 8 variables are ordered.

.CIRCUIT This card signifies the beginning of the circuit description. The next section shows how to fill the .CIRCUIT block with the element descriptions. The arrangement of these descriptions is absolutely free, i.e. mixing of voltage sources and building blocks are allowed.

.INIT This card is needed directly after the input circuit description, if one or more nodal voltages are not defined at the beginning of the simulation. The program verifies the circuit and monitors each undefined nodal or notifies the user, that a short between two or more outputs exist. In the case of undefined initial nodal voltages, the .INIT card helps the program to find these voltages in order to compute the output nodals of each building block. If a constant nodal value of 1E6 occurs, this nodal has not been detected in the element lists, or else the program could not compute this nodal.

In this block, the following declaration is used :

.INIT

Nodal-number Voltage-value ...

.PRINT The next line following .PRINT defines the output declaration:

OUTPUT X or H(nodal) or L(nodal) V(nodalx)...V(nodaly)

X means, that each time step is monitored and the values of each nodal is outputted.

H(nodal-number) or L(nodal-number) means, that during the High -H- or Low -L- level of the nodal, the computed nodal values are written to the file. This enables the user to monitor only the nodal values required to examine the circuit within its active time-window.

.LIMIT The number of the following line limits the number of simulated time steps.

.END This is the last command, used to exit the program and to close all files.

4. Element Syntax Description

There are 20 different elements built in the program. These elements are split into analogue and digital building blocks, so that a mixed mode simulation can be processed. The element description includes a lot of parameters, thus the building blocks can be widely used for many applications. The following abbreviations are used for the element identification.

1. COM comparator
2. AMP amplifier
3. SAM symmetrical single ended amplifier
4. OPA operational amplifier
5. DAM fully differential amplifier
6. DIN fully differential integrator
7. INT integrator
8. DIF differentiator

9. VIS voltage inverter switch
10. SUM 2-terminal summation
11. INV inverter
12. DEL delay
13. SWI 2-terminal input to 1-terminal output switch
14. DSW 1-terminal input to 2-terminal output switch
15. DFF D-flip flop
16. S4R 4-BIT shift register (analogue and digital)
17. NAN 2-input NAND
18. NOR 2-input NOR
19. MUL 2-input multiplier
20. NOI noise (not yet implemented!)
21. XOR 2-input XOR

The following listing shows the terminal declaration of the building blocks.

COM	In	Ref	Out	Hys	Off	Clk							
AMP	In-		Out		Off	Clk		Cin		Cio		Cfth	A
SAM	In-	Ref	Out		Off	Clk		Cin		Cio		Cfth	A
OPA	In-	In+	Out		Off	Clk		Cin		Cio		Cfth	A
DAM	In-	In+	Out+	Out-	Off	Clk		Cin+	Cin-	Cio+	Cio-	Cfth	A
DIN	In-	In+	Out+	Out-	Off	Clk	Clko	Cin+	Cin-	Cio+	Cio-	Cfth	A
INT	In		Out		Off	Clk	Clko	Cin		Cio		Cfth	A
DIF	In		Out			Clk	Clko						
VIS	In		Out			Clk	Clko	C0		C1		Cfth	
SUM	In1	In2	Out										
INV	In		Out		Off								
DEL	In		Out			Clk	Clko						
SWI	In1	In2	Out			Clk							
DSW	In		Out1	Out2		Clk							
DFF	In		Out			Clk							
S4R	In	Out	Out2	Out3	Out4								
NAN	In1	In2	Out										

NOR In1 In2 Out

MUL In In2 Out

XOR In1 In2 Out

The capacitance values used to identify Cin, Ci/o and Cft are unit free, they are simply relations used to compute the element characteristics. The gain A is in the Vout/Vin declaration. Exponentially written numbers are valid.

The Clk terminal is the auto zero input. A nodal voltage above midpoint voltage signs HIGH, below midpoint voltage, the Clk detects low. High means auto zero.

The Clk,(in;out) are the input/output clocks. When the clock is high, the appropriate input/output is active.

Clk,in or Clk,out means that during the High-period of the clock, the nodal information is put in the element or the nodal information is outputted.

The Hysteresis (Hys) of a comparator is the range of the voltage inaccuracy.

The circuit drawings of the library elements are shown in the appendix.

The following identifications are used to control the simulation.

RAS raster

PER period (default 1)

VIN input voltage

VOL supply voltage

The raster defines the sample rate in time units. Within each raster step, the circuits can react on clock pulses. Each clocked circuit reacts only once during its active period. Therefore a multiple clock phase scheme offers a wide range of simulation possibilities. Hence high sophisticated circuits, like Delta Sigma A/D converters can be simulated as well as their digital control unit. The RAS command must be followed by a number that gives the number of rasters during one period.

The period card defines the number of periods to be simulated. The definition of a period is dependent on the circuit. In the case of an A/D converter, the raster is the clock rate of the digit detection process (oversampling or other techniques like successive approximation) and the period is the time in which the A/D process is finished.

The voltage cards are split into VIN and VOL. Up to 50 VIN cards can be used within one simulation. Therefore clock generators are easy to construct. The VIN card itself is split into three arrangements, The LIN, SIN and CON. Therefore most of the voltage shapes can be constructed using these cards. The VIN card arrangement is defined by:

VIN LIN Vmin Vmax No of Subperiods Nodal Delay.Start
VIN SIN Amplitude Voff No of Subperiods Nodal Phase.Start
VIN CON Amplitude Voff No of Subperiods.Duty Nodal Delay.Start

These input voltage cards may be described mathematically as follows:

1. VIN LIN

If Start = 0

V lin = Vmin + (Vmax-Vmin) * (No of subperiods) / Raster

If Start = 1

V Lin = Vmax - (Vmax-Vmin) * (No of subperiods) / Raster

2. VIN SIN

If Start = 1: function is sin

If Start = 0: function is cos

V sin = Amplitude * sin (Step * (2 * pi / Raster) * No of subperiods + Phase) + Voff

where: Step is the number of raster steps.

3. VIN CON

If Start = 1: start with: Vst = Amplitude + Voff

If Start = 0: start with: Vst = Voff

The .DUTY number gives the duty cycle in % of one clock period

The VOL card is the supply voltage definition.

VOL Vpositive Vnegative

This card is used to terminate the output voltage in active elements. Therefore the elements are not based on special processes. Nodal 0 is fixed to 0V. All voltage values are related to 0V.

5. Hints to use the program

Large programs can easily be tested by using the .LIMIT card. This card enables the user to check the simulation under "real" conditions before starting a long time

simulation. The program has about 55 different error messages, so most errors are detected and monitored. There is no need for a special input-file arrangement. The user is completely free to arrange the element descriptions after the .CIRCUIT card. The program checks the ability to compute all of the nodals. Nodals, which cannot be computed are detected and relayed to the user in the .SOU file. In this case no simulation will be performed. The user is informed by a message, that nodals xx to yy need a initialisation by using the .INIT card or that perhaps one or more nodals are connected to more than one output. After succsessful completion of the check routine, the simulation can run properly. The simulation will not be stopped, if a nodal in the output card is invoked, that is not a member of the circuit nodal list. This undefined nodal is not registered as a fault, but a constant number of 1E6 volt will be written in the output list. After completion of the simulation, the results can be graphically seen by using the TPLOT program, or the ASCII file can be studied. The binary output file .SPL can be analysed by the multiradix FFT program MURF. The following examples show a Delta Sigma A to D converter as an input file, an extract of the ASCII output file and the plot produced by the TPLOT package using a HP7475A plotter.

5.1. Example of an input file

```
.TITLE DELTA SIGMA CONVERTER  VIN = 2.3V
.TITLE THE INPUT VOLTAGE IS DIRECTLY USED AS THE COMPARATOR'S
REFERENCE
.TITLE W.TENTEN  24.03.1989
.CIRCUIT

SUM   1  6  2
INTEG 2    3     0 11 9  1  3 0  1E4
COMP  3  1  4  1E-3 0   9        1E4
```

```
DELAY 4  5        10 9
SWIT  7  8 6  5
RASTER 400

$ VOLTAGE SOURCES
$      AMPL VOFF   PERI/DUTY CONNECT HIGH/LOW

VIN CON  2.3  0     1.999     1     0.1
VIN CON  5   -2.5   125.5     9     1.1
VIN CON  5   -2.5   125.5     10     0.1
VIN CON  5   -2.5   1.005     11     0.1
VIN CON  5   -2.5   1.999     7     0.1
VIN CON  5   -2.5   1.999     8     0.0

VOLT 2.5 -2.5

.INIT
5 -2.5

.PRINT
OUTPUT X 1 2 3 4 5 9 10 6 7 8  11
.END
```

5.2 Part of the ASCII output file

```
.TITLE DELTA SIGMA CONVERTER  VIN = 2.3V
.TITLE THE INPUT VOLTAGE IS DIRECTLY USED AS THE COMPARATOR'S
```

REFERENCE

```
.TITLE W.TENTEN  24.03.1989
.CIRCUIT

SUM1   6  2
INTEG2     3      0 11 9  1  3 01E4
COMP3   1  4  1E-3 0   91E4
DELAY4   5 10 9
SWIT7   8  6   5
RASTER 400

$ VOLTAGE SOURCES
$       AMPL VOFF   PERI/DUTY CONNECT HIGH/LOW

VIN CON  2.30      1.999  1 0.1
VIN CON  5   -2.5    125.5  9 1.1
VIN CON  5   -2.5    125.5 10 0.1
VIN CON  5   -2.5     1.005 11 0.1
VIN CON  5   -2.5     1.999  7 0.1
VIN CON  5   -2.5     1.999  8 0.0

VOLT 2.5 -2.5

.INIT
5 -2.5

.PRINT
OUTPUT X 1 2 3 4 5 9 10 6 7 811
```

****** START OF SC - CIRCUIT SIMULATION (V2.3a) ******

FILE TO BE SIMULATED:DSIG14

DATE: 23. 9.1989

TIME: 12:24:37

****** END OF SC - CIRCUIT SIMULATION ******

CPU - TIME USED: 36.14 SECONDS

SC V2.3 GAMMERTINGEN 22.04.1989

DELTA SIGMA CONVERTER VIN = 2.3V

THE INPUT VOLTAGE IS DIRECTLY USED AS THE COMPARATOR'S REFERENCE

W.TENTEN 24.03.1989

TIME	V(1)	V(2)	V(3)	V(4)	V(5)	V(9)	V(10)
1.0000	2.3000	-.20000	.00000	.00000	-2.5000	2.5000	2.5000
2.0000	2.3000	-.20000	.66658E-01	.00000	.00000	2.5000	-2.5000
3.0000	2.3000	2.5000	.66658E-01	-2.5000	.00000	-2.5000	2.5000
4.0000	2.3000	2.5000	.66658E-01	-2.5000	.00000	-2.5000	2.5000
5.0000	2.3000	2.5000	-.76656	.00000	-2.5000	2.5000	-2.5000
6.0000	2.3000	-.20000	-.76656	-2.5000	-2.5000	-2.5000	-2.5000
7.0000	2.3000	-.20000	-.76656	-2.5000	-2.5000	-2.5000	2.5000
8.0000	2.3000	-.20000	-.69991	.00000	-2.5000	2.5000	-2.5000
9.0000	2.3000	-.20000	-.69991	-2.5000	-2.5000	-2.5000	-2.5000
10.000	2.3000	-.20000	-.69991	-2.5000	-2.5000	-2.5000	2.5000

11.000	2.3000	-.20000	-.63325	.00000	-2.5000	2.5000	-2.5000
12.000	2.3000	-.20000	-.63325	-2.5000	-2.5000	-2.5000	-2.5000
13.000	2.3000	-.20000	-.63325	-2.5000	-2.5000	-2.5000	2.5000
14.000	2.3000	-.20000	-.56659	.00000	-2.5000	2.5000	-2.5000
15.000	2.3000	-.20000	-.56659	-2.5000	-2.5000	-2.5000	-2.5000
16.000	2.3000	-.20000	-.56659	-2.5000	-2.5000	-2.5000	2.5000
17.000	2.3000	-.20000	-.49993	.00000	-2.5000	2.5000	-2.5000

.

.

397.00	2.3000	2.5000	1.5998	-2.5000	2.5000	-2.5000	2.5000
398.00	2.3000	2.5000	.76657	.00000	-2.5000	2.5000	-2.5000
399.00	2.3000	-.20000	.76657	-2.5000	-2.5000	-2.5000	-2.5000
400.00	.00000	2.5000	.76657	2.5000	-2.5000	-2.5000	2.5000

SC V2.3 GAMMERTINGEN 22.04.1989

DELTA SIGMA CONVERTER VIN = 2.3V

THE INPUT VOLTAGE IS DIRECTLY USED AS THE COMPARATOR'S REFERENCE

W.TENTEN 24.03.1989

TIME	V(6)	V(7)	V(8)	V(11)
1.0000	-2.5000	2.5000	-2.5000	2.5000
2.0000	-2.5000	2.5000	-2.5000	-2.5000
3.0000	2.5000	2.5000	-2.5000	-2.5000
4.0000	2.5000	2.5000	-2.5000	-2.5000
5.0000	2.5000	2.5000	-2.5000	-2.5000
6.0000	-2.5000	2.5000	-2.5000	-2.5000

7.0000 -2.5000 2.5000 -2.5000 -2.5000

8.0000 -2.5000 2.5000 -2.5000 -2.5000

9.0000 -2.5000 2.5000 -2.5000 -2.5000

10.000 -2.5000 2.5000 -2.5000 -2.5000

11.000 -2.5000 2.5000 -2.5000 -2.5000

12.000 -2.5000 2.5000 -2.5000 -2.5000

13.000 -2.5000 2.5000 -2.5000 -2.5000

14.000 -2.5000 2.5000 -2.5000 -2.5000

15.000 -2.5000 2.5000 -2.5000 -2.5000

16.000 -2.5000 2.5000 -2.5000 -2.5000

17.000 -2.5000 2.5000 -2.5000 -2.5000

.

.

397.00 2.5000 2.5000 -2.5000 -2.5000

398.00 2.5000 2.5000 -2.5000 -2.5000

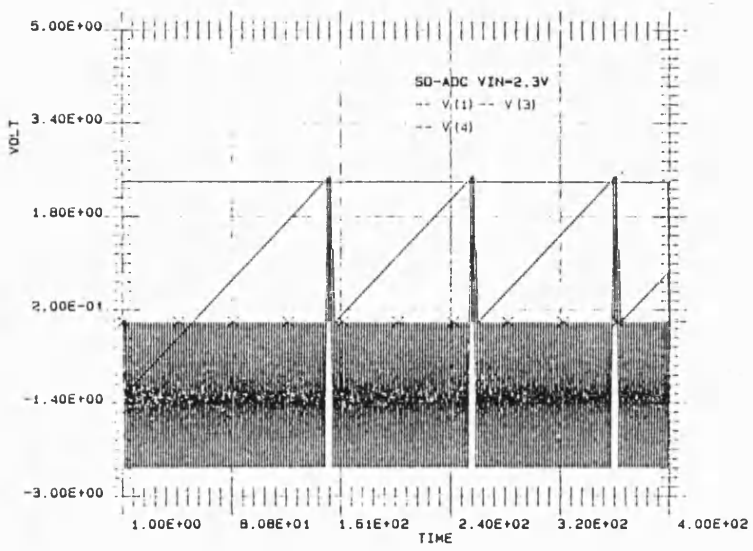
399.00 -2.5000 2.5000 -2.5000 -2.5000

400.00 2.5000 -2.5000 2.5000 -2.5000

.END

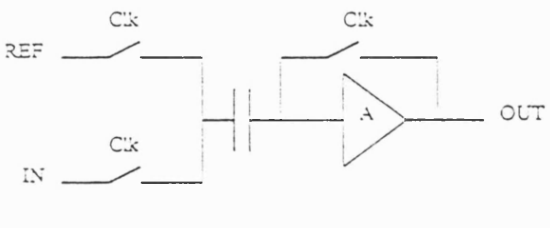
SIMULATION - TIME USED: 52.12 SECONDS

5.3 TPLOT output

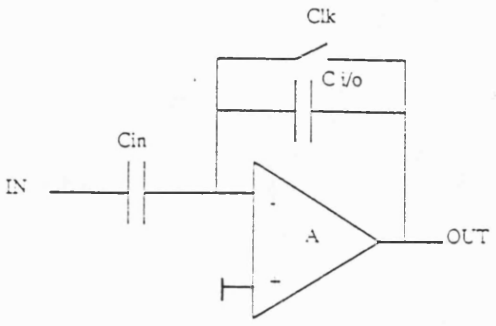


TPLOT output of Sigma Delta ADC

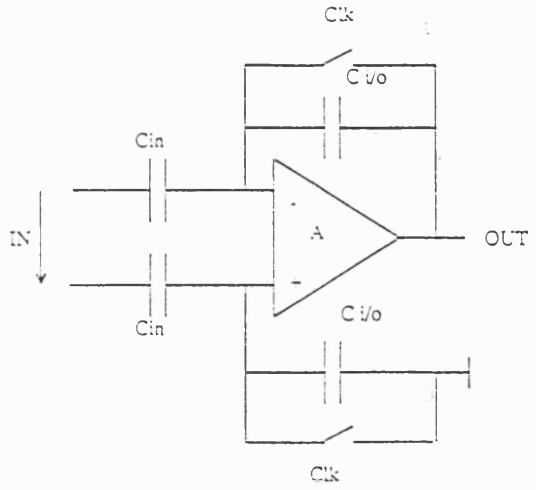
5.4 Circuit building block drawings



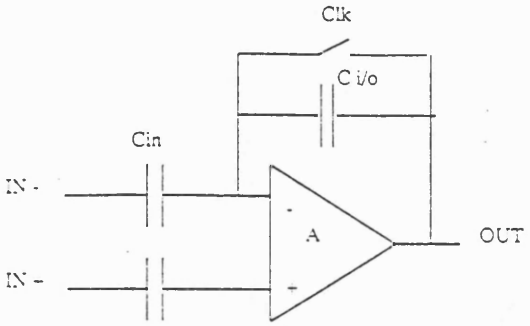
COMPARATOR (COM)



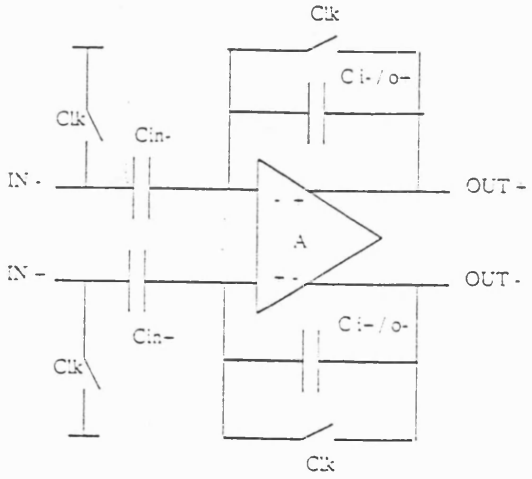
AMPLIFIER (AMP)



S-AMPLIFIER (SAM)

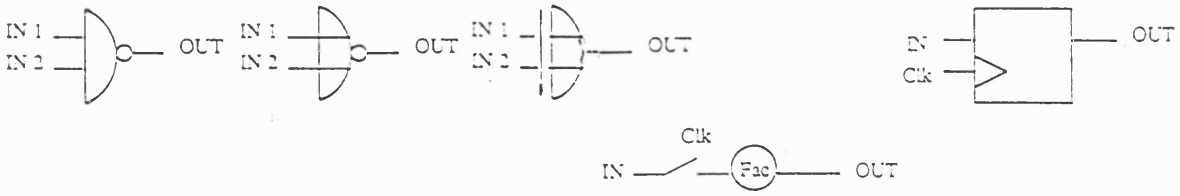


OPERATIONAL AMPLIFIER (OPA)

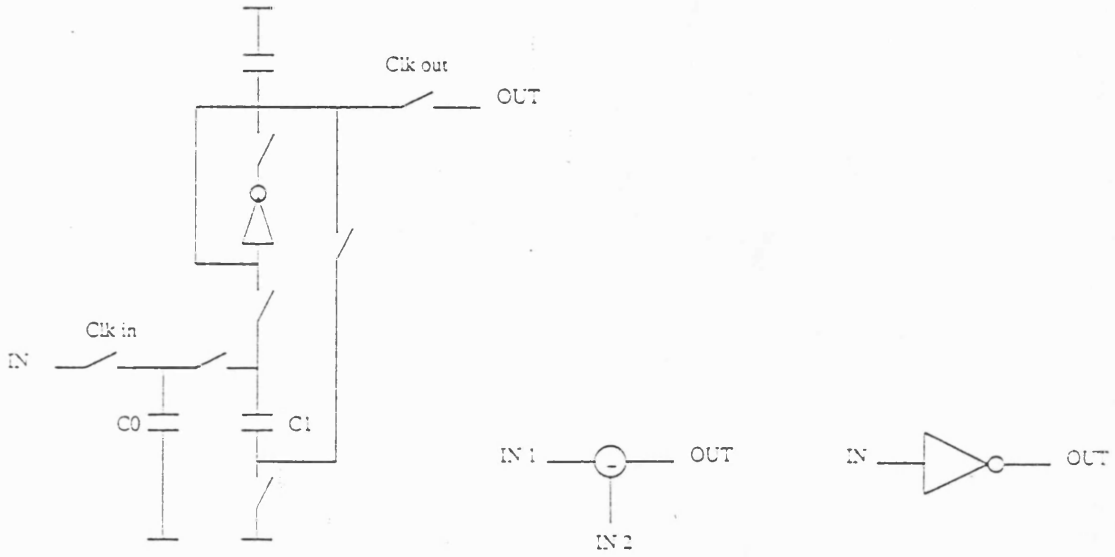


FULLY DIFF. OPAMP (DAM)

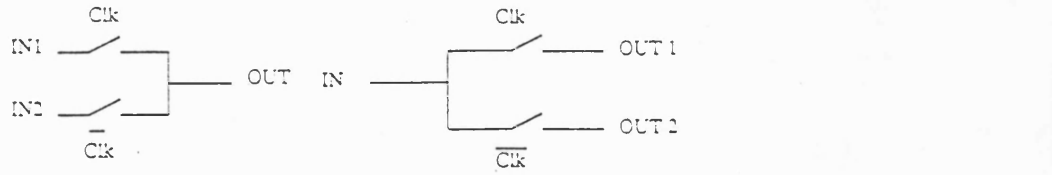
FULLY DIFF. INTEGRATOR (DIN)



NAND NOR XOR MULTIPLIER (MUL) D-FLIP-FLOP (DFF)



VOLTAGE INVERTER SWITCH (VIS) SUM INVERTER (INV)



DELAY (DEL) SWITCH (SWI) D-SWITCH (DSW) 4-BIT SHIFT REG. (S4R)

APPENDIX V

CLOCK-FEED-THROUGH SENSITIVITY OF THE AC-CROSS COUPLED COMPARATOR

```
.TITLE AC-CROSS COUPLED COMPARATOR
.TITLE W.TENTEN
.TITLE 10.10.1988
.INCLUDE PARM3U.BO
.INCLUDE INV_TR
.INCLUDE INV_CMP
.INCLUDE TG_GR_TR
.TEMP 25
.CIRCUIT
RIN 10 20 5
XTG_1 20 30 105 115 99 98 TG
CL 30  0 5
XCLK1 100 105 99 98 INV_CL
XCLK2 110 115 99 98 INV_CL
C-CLK1 105 0 2
C-CLK2 115 0 2
VPHI   100 0  5  0 -2.5 80 2 2 300
VPHIN  110 0 -5 10  2.5 60 2 2 300
VIN    10 0  1.000
VDD    99 0  2.5
VSS    98 0 -2.5
.CHECK
ELEMENTS ALL
```

```
.OUTPUT PRINT
V(10) V(20) V(30) I(M1) I(M2)
V(100) V(105) V(110) V(115)
.TRANSIENT MNA 5 0 350
.END
```

Table AV-1 BONSAI input file for the transfer-gate-simulation

TIME	V(10)	V(20)	V(30)	I(M1)	I(M2)	V(100)	V(105)	V(110)	V(115)
.00000s	1.00000V	.00000V	.00000V	.00000A	.00000A	-2.5000V	.00000V	2.50000V	.00000V
5.0000ns	1.00000V	323.27mV	73.137mV	131.20uA	.00000A	2.50000V	-2.4983V	2.50000V	-2.4996V
10.000ns	1.00000V	400.97mV	191.08mV	116.14uA	.00000A	2.50000V	-2.5000V	2.50000V	-2.4996V
15.000ns	1.00000V	1.04616V	274.02mV	.00000A	.00000A	2.50000V	-2.5001V	-2.5000V	2.39174V
20.000ns	1.00000V	1.00034V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.49990V
25.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
30.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
35.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
40.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
45.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
50.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
55.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
60.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
65.000ns	1.00000V	1.00000V	274.30mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
70.000ns	1.00000V	912.68mV	269.90mV	.00000A	.00000A	2.50000V	-2.5001V	2.50000V	808.38mV
75.000ns	1.00000V	490.92mV	322.53mV	98.573uA	.00000A	2.50000V	-2.5000V	2.50000V	-2.4997V
80.000ns	1.00000V	573.97mV	414.00mV	97.432uA	.00000A	-2.5000V	-1.1408V	2.50000V	-2.4995V
85.000ns	1.00000V	584.64mV	519.87mV	40.772uA	39.204uA	-2.5000V	2.49324V	2.50000V	-2.4997V
90.000ns	1.00000V	645.63mV	588.93mV	36.689uA	30.698uA	-2.5000V	2.50041V	2.50000V	-2.4998V
95.000ns	1.00000V	697.92mV	647.61mV	33.299uA	24.166uA	-2.5000V	2.50035V	2.50000V	-2.4998V
100.00ns	1.00000V	742.17mV	697.67mV	30.009uA	19.053uA	-2.5000V	2.50030V	2.50000V	-2.4998V
105.00ns	1.00000V	779.68mV	740.44mV	26.883uA	15.054uA	-2.5000V	2.50025V	2.50000V	-2.4999V
110.00ns	1.00000V	811.53mV	777.01mV	23.960uA	11.925uA	-2.5000V	2.50022V	2.50000V	-2.4999V
115.00ns	1.00000V	838.62mV	808.31mV	21.260uA	9.4763uA	-2.5000V	2.50018V	2.50000V	-2.4999V
120.00ns	1.00000V	861.68mV	835.14mV	18.794uA	7.5566uA	-2.5000V	2.50016V	2.50000V	-2.4999V
125.00ns	1.00000V	881.35mV	858.14mV	16.560uA	6.0491uA	-2.5000V	2.50013V	2.50000V	-2.4999V
130.00ns	1.00000V	898.14mV	877.89mV	14.550uA	4.8624uA	-2.5000V	2.50012V	2.50000V	-2.4999V
135.00ns	1.00000V	912.50mV	894.85mV	12.753uA	3.9255uA	-2.5000V	2.50010V	2.50000V	-2.4999V

140.00ns 1.00000V 924.79mV 909.42mV 11.155uA 3.1834uA -2.5000V 2.50008V 2.50000V -2.5000V

145.00ns 1.00000V 935.31mV 921.95mV 9.7399uA 2.5934uA -2.5000V 2.50007V 2.50000V -2.5000V

150.00ns 1.00000V 944.34mV 932.74mV 8.4909uA 2.1223uA -2.5000V 2.50006V 2.50000V -2.5000V

155.00ns 1.00000V 952.09mV 942.02mV 7.3921uA 1.7446uA -2.5000V 2.50005V 2.50000V -2.5000V

160.00ns 1.00000V 958.74mV 950.01mV 6.4281uA 1.4404uA -2.5000V 2.50005V 2.50000V -2.5000V

165.00ns 1.00000V 964.46mV 956.89mV 5.5842uA 1.1942uA -2.5000V 2.50004V 2.50000V -2.5000V

170.00ns 1.00000V 969.38mV 962.82mV 4.8469uA 993.97nA -2.5000V 2.50003V 2.50000V -2.5000V

175.00ns 1.00000V 973.61mV 967.93mV 4.2038uA 830.42nA -2.5000V 2.50003V 2.50000V -2.5000V

180.00ns 1.00000V 977.25mV 972.33mV 3.6437uA 696.19nA -2.5000V 2.50003V 2.50000V -2.5000V

185.00ns 1.00000V 980.38mV 976.13mV 3.1564uA 585.53nA -2.5000V 2.50002V 2.50000V -2.5000V

190.00ns 1.00000V 983.09mV 979.41mV 2.7330uA 493.90nA -2.5000V 2.50002V 2.50000V -2.5000V

195.00ns 1.00000V 985.41mV 982.23mV 2.3655uA 417.73nA -2.5000V 2.50002V 2.50000V -2.5000V

200.00ns 1.00000V 987.42mV 984.67mV 2.0466uA 354.16nA -2.5000V 2.50001V 2.50000V -2.5000V

205.00ns 1.00000V 989.14mV 986.77mV 1.7702uA 300.91nA -2.5000V 2.50001V 2.50000V -2.5000V

210.00ns 1.00000V 990.63mV 988.58mV 1.5307uA 256.17nA -2.5000V 2.50001V 2.50000V -2.5000V

215.00ns 1.00000V 991.92mV 990.14mV 1.3233uA 218.45nA -2.5000V 2.50001V 2.50000V -2.5000V

220.00ns 1.00000V 993.03mV 991.49mV 1.1437uA 186.58nA -2.5000V 2.50001V 2.50000V -2.5000V

225.00ns 1.00000V 993.98mV 992.66mV 988.39nA 159.57nA -2.5000V 2.50001V 2.50000V -2.5000V

230.00ns 1.00000V 994.81mV 993.66mV 854.03nA 136.64nA -2.5000V 2.50001V 2.50000V -2.5000V

235.00ns 1.00000V 995.52mV 994.53mV 737.83nA 117.12nA -2.5000V 2.50001V 2.50000V -2.5000V

240.00ns 1.00000V 996.13mV 995.28mV 637.38nA 100.49nA -2.5000V 2.50000V 2.50000V -2.5000V

245.00ns 1.00000V 996.66mV 995.92mV 550.54nA 86.282nA -2.5000V 2.50000V 2.50000V -2.5000V

250.00ns 1.00000V 997.12mV 996.48mV 475.50nA 74.139nA -2.5000V 2.50000V 2.50000V -2.5000V

255.00ns 1.00000V 997.51mV 996.96mV 410.66nA 63.744nA -2.5000V 2.50000V 2.50000V -2.5000V

260.00ns 1.00000V 997.85mV 997.38mV 354.64nA 54.835nA -2.5000V 2.50000V 2.50000V -2.5000V

265.00ns 1.00000V 998.15mV 997.74mV 306.24nA 47.194nA -2.5000V 2.50000V 2.50000V -2.5000V

270.00ns 1.00000V 998.40mV 998.05mV 264.44nA 40.634nA -2.5000V 2.50000V 2.50000V -2.5000V

275.00ns 1.00000V 998.62mV 998.31mV 228.34nA 34.998nA -2.5000V 2.50000V 2.50000V -2.5000V

280.00ns 1.00000V 998.81mV 998.54mV 197.15nA 30.153nA -2.5000V 2.50000V 2.50000V -2.5000V

285.00ns 1.00000V 998.97mV 998.74mV 170.22nA 25.986nA -2.5000V 2.50000V 2.50000V -2.5000V

290.00ns 1.00000V 999.11mV 998.92mV 146.97nA 22.399nA -2.5000V 2.50000V 2.50000V -2.5000V

295.00ns 1.00000V 999.23mV 999.06mV 126.89nA 19.312nA -2.5000V 2.50000V 2.50000V -2.5000V

300.00ns 1.00000V 999.34mV 999.19mV 109.55nA 16.653nA -2.5000V 2.50000V 2.50000V -2.5000V

305.00ns 1.00000V 986.24mV 983.00mV 2.4102uA .00000A 2.50000V -2.4959V 2.50000V -2.5000V

310.00ns 1.00000V 988.31mV 985.28mV 2.2529uA .00000A 2.50000V -2.5000V 2.50000V -2.5000V

315.00ns 1.00000V 1.07477V 1.04089V .00000A .00000A 2.50000V -2.5001V -2.5000V 2.39057V

320.00ns 1.00000V 1.00047V 1.04117V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.49990V

325.00ns 1.00000V 1.00000V 1.04117V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

330.00ns 1.00000V 1.00000V 1.04117V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

335.00ns 1.00000V 1.00000V 1.04117V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

340.00ns 1.00000V 1.00000V 1.04117V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

345.00ns 1.00000V 1.00000V 1.04117V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

350.00ns 1.00000V 1.00000V 1.04117V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

BONSAI V1.2c (GAMMERTINGEN 26.06.88)

Table AV-2 BONSAI ASCII output file for CL=5pF

TIME	V(10)	V(20)	V(30)	I(M1)	I(M2)	V(100)	V(105)	V(110)	V(115)
.00000s	1.00000V	.00000V	.00000V	.00000A	.00000A	-2.5000V	.00000V	2.50000V	.00000V
5.0000ns	1.00000V	373.48mV	159.58mV	116.56uA	.00000A	2.50000V	-2.4983V	2.50000V	-2.4991V
10.000ns	1.00000V	530.51mV	385.51mV	87.033uA	.00000A	2.50000V	-2.4999V	2.50000V	-2.4993V
15.000ns	1.00000V	1.05316V	563.35mV	.00000A	.00000A	2.50000V	-2.5001V	-2.5000V	2.39183V
20.000ns	1.00000V	1.00037V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.49990V
25.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
30.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
35.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
40.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
45.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
50.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
55.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
60.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
65.000ns	1.00000V	1.00000V	564.02mV	.00000A	.00000A	2.50000V	-2.5000V	-2.5000V	2.50000V
70.000ns	1.00000V	912.68mV	553.57mV	.00000A	.00000A	2.50000V	-2.5001V	2.50000V	808.35mV
75.000ns	1.00000V	678.71mV	587.30mV	59.349uA	.00000A	2.50000V	-2.4999V	2.50000V	-2.4995V
80.000ns	1.00000V	786.89mV	708.48mV	53.280uA	.00000A	-2.5000V	-1.1393V	2.50000V	-2.4994V
85.000ns	1.00000V	849.08mV	821.08mV	19.730uA	8.1933uA	-2.5000V	2.49317V	2.50000V	-2.4998V
90.000ns	1.00000V	891.63mV	871.47mV	14.450uA	4.9912uA	-2.5000V	2.50028V	2.50000V	-2.4998V
95.000ns	1.00000V	922.25mV	907.32mV	10.826uA	3.1331uA	-2.5000V	2.50020V	2.50000V	-2.4999V
100.00ns	1.00000V	944.08mV	933.09mV	8.0364uA	2.0091uA	-2.5000V	2.50014V	2.50000V	-2.4999V
105.00ns	1.00000V	959.70mV	951.65mV	5.9258uA	1.3158uA	-2.5000V	2.50010V	2.50000V	-2.4999V
110.00ns	1.00000V	970.92mV	965.04mV	4.3483uA	878.79nA	-2.5000V	2.50007V	2.50000V	-2.5000V
115.00ns	1.00000V	978.99mV	974.71mV	3.1795uA	597.13nA	-2.5000V	2.50005V	2.50000V	-2.5000V
120.00ns	1.00000V	984.81mV	981.69mV	2.3189uA	411.69nA	-2.5000V	2.50004V	2.50000V	-2.5000V
125.00ns	1.00000V	989.02mV	986.75mV	1.6882uA	287.21nA	-2.5000V	2.50003V	2.50000V	-2.5000V
130.00ns	1.00000V	992.05mV	990.40mV	1.2273uA	202.25nA	-2.5000V	2.50002V	2.50000V	-2.5000V
135.00ns	1.00000V	994.25mV	993.05mV	891.40nA	143.46nA	-2.5000V	2.50001V	2.50000V	-2.5000V
140.00ns	1.00000V	995.83mV	994.97mV	646.97nA	102.32nA	-2.5000V	2.50001V	2.50000V	-2.5000V
145.00ns	1.00000V	996.98mV	996.35mV	469.32nA	73.276nA	-2.5000V	2.50001V	2.50000V	-2.5000V
150.00ns	1.00000V	997.82mV	997.36mV	340.33nA	52.640nA	-2.5000V	2.50001V	2.50000V	-2.5000V
155.00ns	1.00000V	998.42mV	998.09mV	246.72nA	37.901nA	-2.5000V	2.50000V	2.50000V	-2.5000V
160.00ns	1.00000V	998.85mV	998.61mV	178.83nA	27.335nA	-2.5000V	2.50000V	2.50000V	-2.5000V

165.00ns 1.00000V 999.17mV 999.00mV 129.60nA 19.738nA -2.5000V 2.50000V 2.50000V -2.5000V

170.00ns 1.00000V 999.40mV 999.27mV 93.913nA 14.265nA -2.5000V 2.50000V 2.50000V -2.5000V

175.00ns 1.00000V .99956V 999.47mV 68.049nA 10.317nA -2.5000V 2.50000V 2.50000V -2.5000V

180.00ns 1.00000V .99968V .99962V 49.305nA 7.4646nA -2.5000V 2.50000V 2.50000V -2.5000V

185.00ns 1.00000V .99977V .99972V 35.722nA 5.4028nA -2.5000V 2.50000V 2.50000V -2.5000V

190.00ns 1.00000V .99983V .99980V 25.881nA 3.9115nA -2.5000V 2.50000V 2.50000V -2.5000V

195.00ns 1.00000V .99988V .99985V 18.750nA 2.8323nA -2.5000V 2.50000V 2.50000V -2.5000V

200.00ns 1.00000V .99991V .99989V 13.584nA 2.0511nA -2.5000V 2.50000V 2.50000V -2.5000V

205.00ns 1.00000V .99994V .99992V 9.8411nA 1.4856nA -2.5000V 2.50000V 2.50000V -2.5000V

210.00ns 1.00000V .99995V .99994V 7.1295nA 1.0760nA -2.5000V 2.50000V 2.50000V -2.5000V

215.00ns 1.00000V .99997V .99996V 5.1650nA 779.41pA -2.5000V 2.50000V 2.50000V -2.5000V

220.00ns 1.00000V .99998V .99997V 3.7418nA 564.58pA -2.5000V 2.50000V 2.50000V -2.5000V

225.00ns 1.00000V .99998V .99998V 2.7107nA 408.98pA -2.5000V 2.50000V 2.50000V -2.5000V

230.00ns 1.00000V .99999V .99998V 1.9638nA 296.27pA -2.5000V 2.50000V 2.50000V -2.5000V

235.00ns 1.00000V .99999V .99999V 1.4227nA 214.62pA -2.5000V 2.50000V 2.50000V -2.5000V

240.00ns 1.00000V .99999V .99999V 1.0306nA 155.48pA -2.5000V 2.50000V 2.50000V -2.5000V

245.00ns 1.00000V 1.00000V .99999V 746.65pA 112.63pA -2.5000V 2.50000V 2.50000V -2.5000V

250.00ns 1.00000V 1.00000V 1.00000V 540.91pA 81.596pA -2.5000V 2.50000V 2.50000V -2.5000V

255.00ns 1.00000V 1.00000V 1.00000V 391.86pA 59.111pA -2.5000V 2.50000V 2.50000V -2.5000V

260.00ns 1.00000V 1.00000V 1.00000V 283.88pA 42.823pA -2.5000V 2.50000V 2.50000V -2.5000V

265.00ns 1.00000V 1.00000V 1.00000V 205.66pA 31.023pA -2.5000V 2.50000V 2.50000V -2.5000V

270.00ns 1.00000V 1.00000V 1.00000V 148.99pA 22.474pA -2.5000V 2.50000V 2.50000V -2.5000V

275.00ns 1.00000V 1.00000V 1.00000V 107.93pA 16.281pA -2.5000V 2.50000V 2.50000V -2.5000V

280.00ns 1.00000V 1.00000V 1.00000V 78.191pA 11.795pA -2.5000V 2.50000V 2.50000V -2.5000V

285.00ns 1.00000V 1.00000V 1.00000V 56.645pA 8.5447pA -2.5000V 2.50000V 2.50000V -2.5000V

290.00ns 1.00000V 1.00000V 1.00000V 41.037pA 6.1901pA -2.5000V 2.50000V 2.50000V -2.5000V

295.00ns 1.00000V 1.00000V 1.00000V 29.729pA 4.4844pA -2.5000V 2.50000V 2.50000V -2.5000V

300.00ns 1.00000V 1.00000V 1.00000V 21.537pA 3.2487pA -2.5000V 2.50000V 2.50000V -2.5000V

305.00ns 1.00000V 973.19mV 966.81mV 4.7188uA .00000A 2.50000V -2.4959V 2.50000V -2.5000V

310.00ns 1.00000V 980.80mV 976.05mV 3.5272uA .00000A 2.50000V -2.5000V 2.50000V -2.5000V

315.00ns 1.00000V 1.07074V 1.10645V .00000A .00000A 2.50000V -2.5001V -2.5000V 2.39023V

320.00ns 1.00000V 1.00045V 1.10712V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.49990V

325.00ns 1.00000V 1.00000V 1.10712V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

330.00ns 1.00000V 1.00000V 1.10712V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

335.00ns 1.00000V 1.00000V 1.10712V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

340.00ns 1.00000V 1.00000V 1.10712V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

345.00ns 1.00000V 1.00000V 1.10712V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

350.00ns 1.00000V 1.00000V 1.10712V .00000A .00000A 2.50000V -2.5000V -2.5000V 2.50000V

BONSAI V1.2c (GAMMERTINGEN 26.06.88)

Table AV-3 BONSAI ASCII output file for CL=2pF

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Novel chopper OTA with dynamic bias control and current controlled cascoded output

W. J. TENTEN† and P. R. SHEPHERD†

A novel monolithic chopper amplifier design is presented. The chopper concept of Coln (1981) is improved using an operational transconductance amplifier (OTA) with dynamic bias and a current controlled cascoded output stage. The low pass filter section of the indirect chopper circuit is realised using switched capacitor circuitry, making the amplifier realizable on silicon.

1. Background

In common use in modern analogue CMOS design is the operational transconductance amplifier (OTA). Improvements in analogue CMOS circuits, especially in the field of analogue-to-digital conversion and switched capacitor circuits, require improved accuracy of the amplifier and comparator stages. An important aspect of these designs is the compensation of the offset voltage. A recent publication (Coln 1981) presented a feed forward offset compensation technique based on the chopper-stabilized principle. We describe in this paper some circuit improvements which may be implemented to improve the performance of circuits based on this technique.

The principle of chopper amplifiers was introduced by Goldberg (1950). There are two basic types of chopper technique: firstly the direct chopper technique, whereby the signal path itself is chopped; and secondly the indirect technique, which uses an additional chopped bypass. The bypass route is connected to the signal path via a low pass filter, cascading the amplification characteristics of the two branches. The chopper technique employed in this work is the indirect one. Indirect chopper compensation is done with time continuous operation of the main amplifier, while the offset compensation is achieved using an auto-zero auxiliary bypass circuit. The resulting offset is chopped into the nulling input of the main amplifier after transition through a low pass filter section, as shown in Fig. 1. For correct operation, both amplifiers must have the same transfer characteristic. The accuracy of the offset compensation is increased with the additional DC amplification of the auxiliary auto-zero amplifier. The signal amplification as well as power supply and common mode rejection ratios (PSRR and CMRR) will be increased by the cascaded amplification of the auxiliary amplifier loop. The characteristic of the auxiliary loop is of course restricted by the characteristic of the low pass filter.

2. Circuit improvements

Improvements in the amplifier can be achieved by the control of the cascode output stage. CMOS OTA designs have been presented (Hosticka 1980) using a

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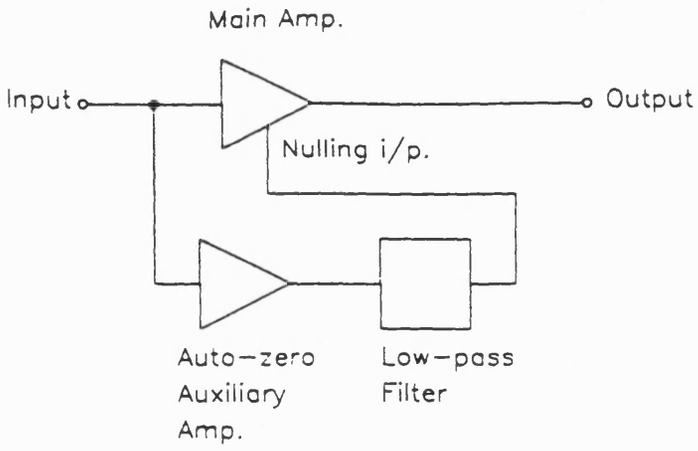


Figure 1. Block diagram of indirect chopper amplifier.

cascode output. The usual method is to control the cascode transistors with a fixed voltage biased to 50% of the supply range. In this paper a new method of controlling the cascode transistors is presented. Here the cascoded transistors act as current controlled current sources, hence the effect of a stacked mirror characteristic is included in this design technique. The current control of the cascode stage is done using a stacked current mirror controlled by the OTA bias source. Figure 2 shows this circuit configuration.

Stacked mirror techniques improve the current stability in respect to supply voltage ringing, due to internal limitation of the drain to source voltage. Although giving improved current stability, the cascode control circuit in Fig. 2 operates with the same backbias voltage drop within the current mirrors at the OTA DC operating point of 50% supply range. To avoid influences of channel length modulation, the current mirror factor should not exceed 10. The accuracy of the current mirror that controls the output cascode depends on the accuracy of the bias source. To decrease the influence of the power supply ringing and to enable this amplifier to be used in designs that force a loadless operation within one cycle, the biasing of the

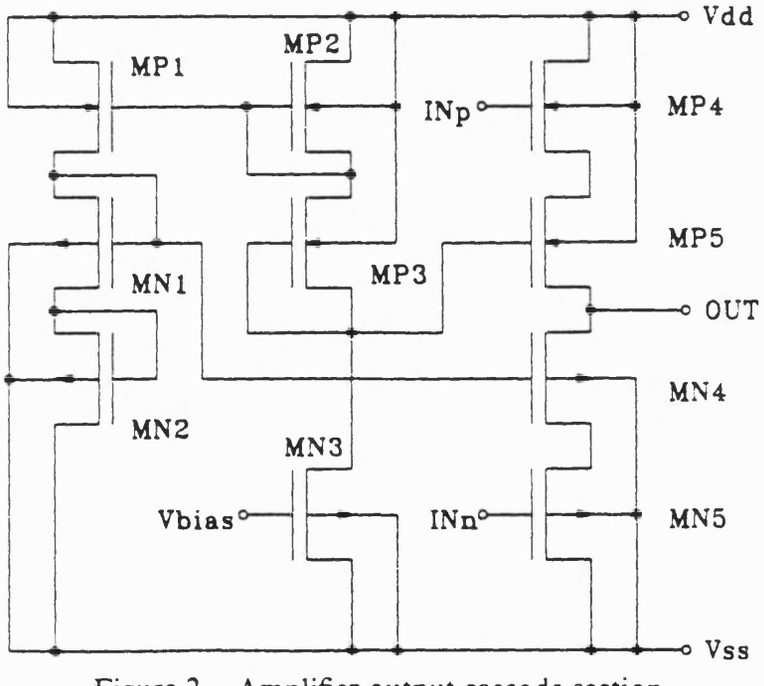


Figure 2. Amplifier output cascode section.

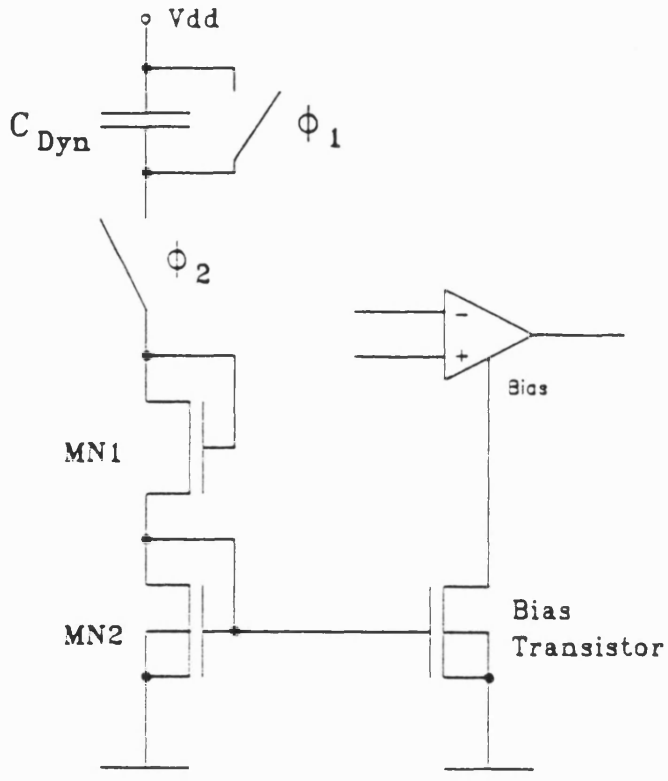


Figure 3. Dynamic bias stage.

amplifiers should be done dynamically. Figure 3 shows a dynamic bias stage. During charge time, the charge current will be mirrored into the bias stage and the cascode control stage. The active time of the amplifier is stongly dependent on the charge or discharge time of the maximum load capacitor. Improvements of the power supply and common mode rejection are strongly dependent on the increased amplification characteristic of the cascaded amplifiers and of the dynamic biasing of the amplifiers. The common mode and power supply rejection ratios are directly related to the amplification factor, so increasing the amplification will improve these ratios.

The nature of dynamic bias control enables the amplifier to act in the active mode for a minimum length of time, during the rest of the bias period the amplifier operates in weak inversion. The amplification is increased within weak inversion due to the decreased bias currents within the amplifier. The output resistance of the cascoded stage is increased as well. Therefore reaction of the amplifier to ringing on the supply line or changing of the input voltages are efficiently damped. The signal frequency is limited by the unity gain frequency of the chopper amplifier and by the desired accuracy of the system.

Figure 4 shows the switched capacitor low pass filter. It has been known since the last century that such a switched capacitor circuit can have the same characteristics as an ohmic resistor. The low pass frequency of the chopper section is very low, so in order to realize the low pass with a standard *RC* combination, the values of the resistor and capacitor would be too big for realization on silicon. The switched capacitor (SC) technique, however, enables the integration of a low pass filter such as this. Care must be taken to avoid clock feedthrough during the auto-zero phase, this can be done by controlling the SC low pass clock with the auto-zero clock.

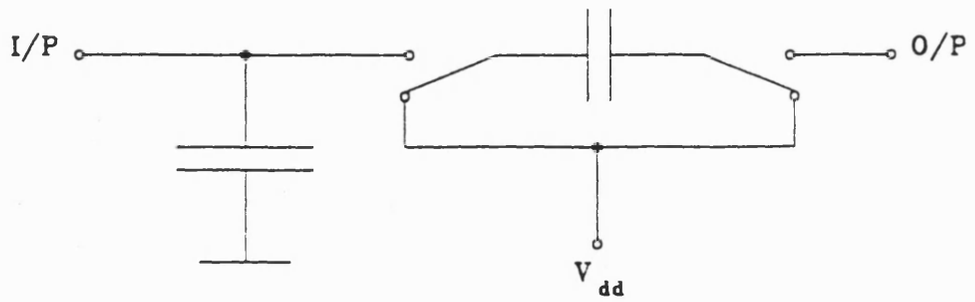


Figure 4. Switched capacitor low pass filter.

Figure 5 shows the circuit of the chopper amplifier. It is to be noted that the auxiliary input of the nulling amplifier is inverting and the auxiliary input of the main amplifier is non-inverting. In order to reduce the influence of the power supply ringing error voltage on the capacitors and leakage current of the capacitors, all of the capacitors should be laid out within their own p-well (n-substrate), or with a hard-wired guard ring (p-substrate). The clocks used for the chopper amplifier presented here must have a non-overlapping characteristic. To minimize the parasitic influences, the top plate of the capacitors must be connected to the inputs of the active devices. The reasons for this are twofold. Firstly, the top plates are further from the bulk of the chip, and hence have lower parasitic capacitance. Secondly they are smaller in area and hence have lower parasitic fringing effects.

3. Simulation results

The simulation tool used in this work is BONSAI (BOsch Network Simulation and Analysis Instrument). BONSAI is a network analysis simulator with parametric model equations. The parameters being used are based on the semiconductor physics of the devices. Analyses can be performed under DC, transient, or AC conditions. Transient simulations are based either on state variable analysis (SVA) or on modified nodal analysis (MNA). SVA operates faster than MNA and is especially

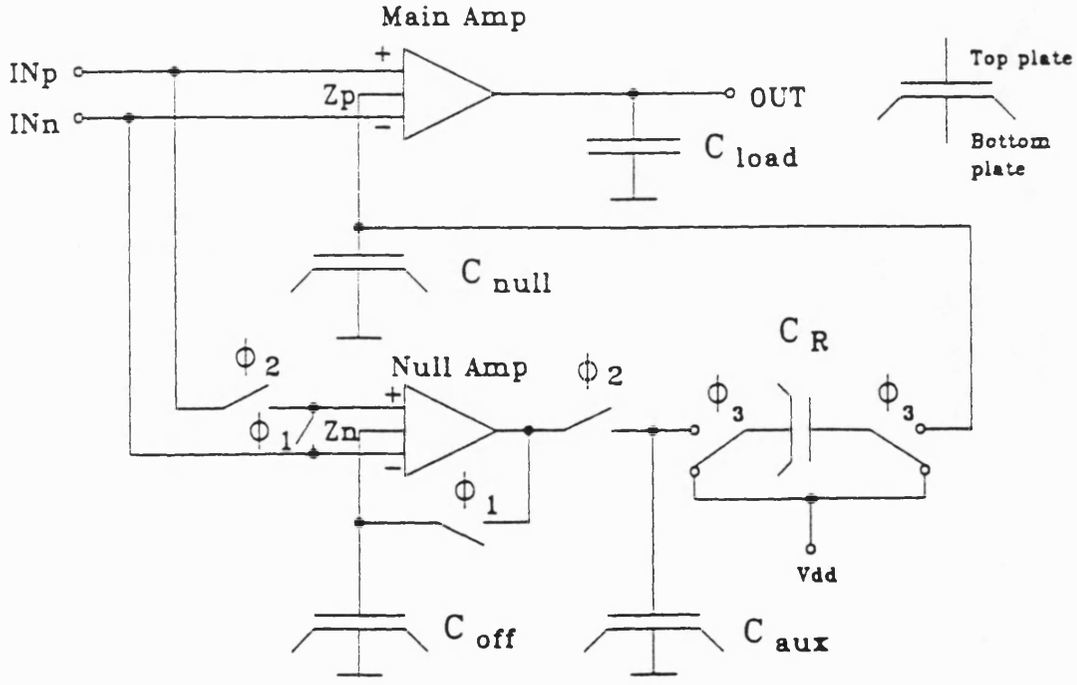


Figure 5. Chopper amplifier.

Parameter	OTA	Null/main OTA	Chopper OTA
Unity gain frequency (MHz)	25	20	20
C_L min (pF)	20	20	20
Phase margin (deg)	15	40	40
Slew rate (C_L min) (V/μsec)	7	7	7
A_0 (dB)	60	59	112
$f_{chopper}(\phi_{1,2})$ (Hz)			500
$f_{SC-R}(\phi_3)$ (Hz)			4000
V_{off}(mV)	<10	<10	$<0{\cdot}05$

Table 1. Simulation results.

applicable for digital simulations. MNA is more useful if the nodes are connected with large conductances and/or capacitors, and the conductances/capacitances to ground are small. It has been found that BONSAI has greater mathematical stability compared to other tools, e.g. SPICE.

BONSAI has an automatic timestep adjustment mechanism, so that the step-width is reduced if any nodal voltage changes faster than a preset error value. Due to this, the simulation times for large circuits can become excessively long. Therefore it is often better to split a particular circuit into several sub-circuits for analysis, and then use the results from one sub-circuit as the initial values for the simulation of the next sub-circuit. This can lead to dramatic savings in cpu time. The simulation of the chopper amplifier presented here was done as a series of sub-circuits. These sub-circuits are described below.

(*a*) OTA. Basic OTA with current controlled cascode but without dynamic biasing.

(*b*) Null/Main OTA. Based on (*a*) but with auxiliary nulling input stage.

(*c*) Chopper OTA. Based on (*b*) with standard *RC* low-pass filter circuit.

(*d*) Bias. Dynamic bias control circuit.

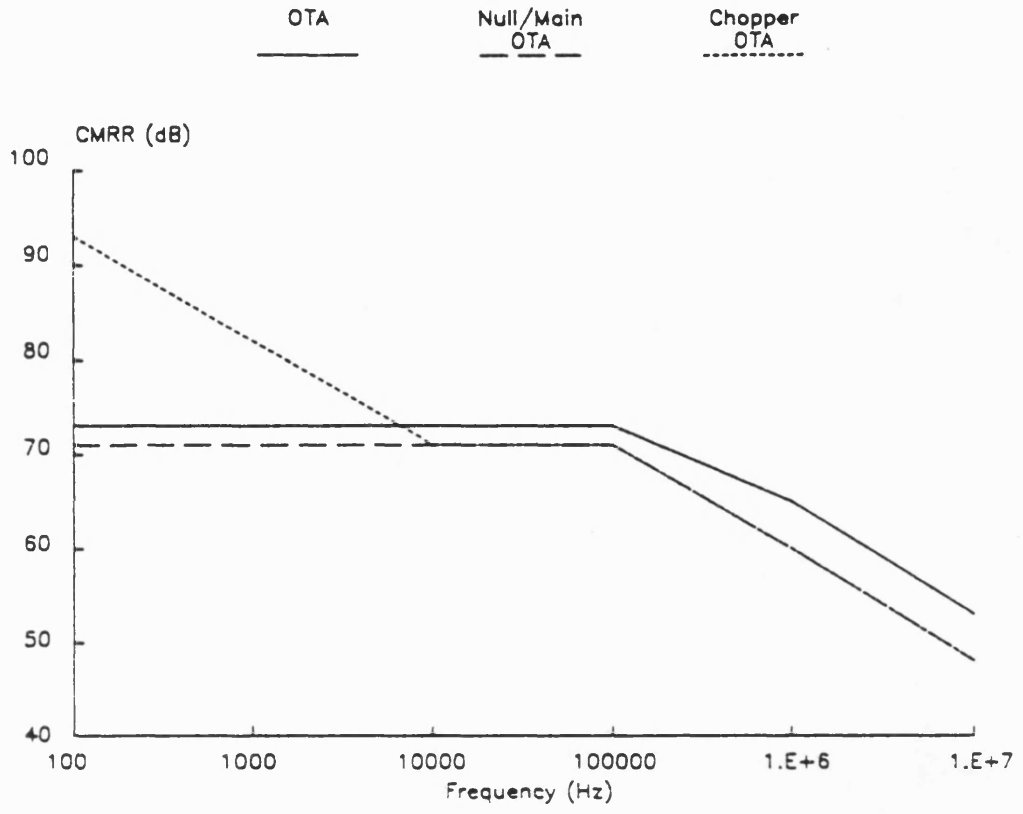
(*e*) Low Pass. SC realization of low pass circuit in (*c*).

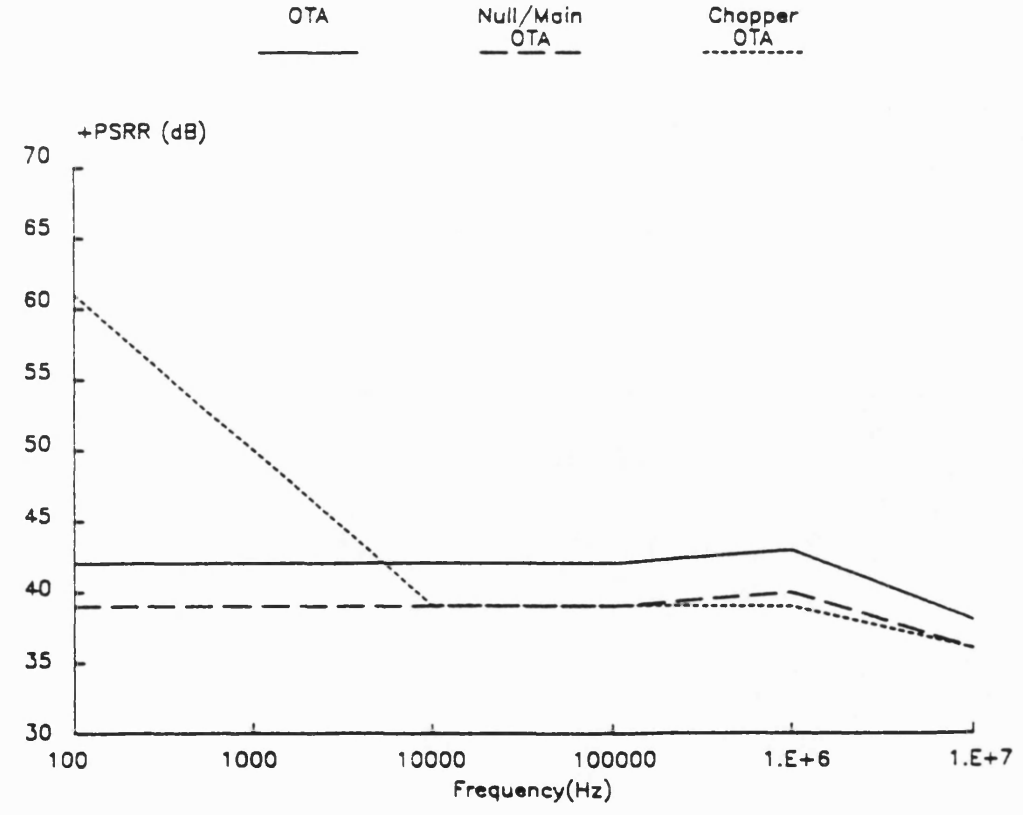
A summary of results of the BONSAI simulations is given in Table 1. The results of the CMRR and PSRR for the positive and negative supply rails are presented in graphical form in Fig. 6.

4. Discussion of results

The design of the chopper OTA presented has been done with a view to the worst case conditions. Care should be taken in the matching of the cascaded amplifiers; assuming the first pole frequency of the nulling amplifier with the low pass filter is bigger than the corner frequency (3 dB) of the main amplifier, the phase margin of the system can severely influence the stability of the low frequency operation. The capacitor C_{null} (Fig. 5) must be big enough to minimize the influence of the clock feedthrough caused by the switching of ϕ_3 low. C_{null} must be in the order of at least 50 pF, using minimum transfer gate geometries and considering the worst case parameter conditions, in order to hold the clock feedthrough offset below 1 mV. In this design the value of C_{null} is 100 pF, C_R is 0·5 pF and the transfer gate has minimum geometries.

The stacked characteristic of this chopper OTA concept is seen in Fig. 6 as an increasing effect below the dominant pole frequency of the auxiliary amplifier. The increase in PSRR just before the roll-off is caused by capacitive coupling within the amplifier. It is to be noted that the OTA requires a minimum value of output load capacitance for correct operation. The minimum value for the design presented here is 20 pF.





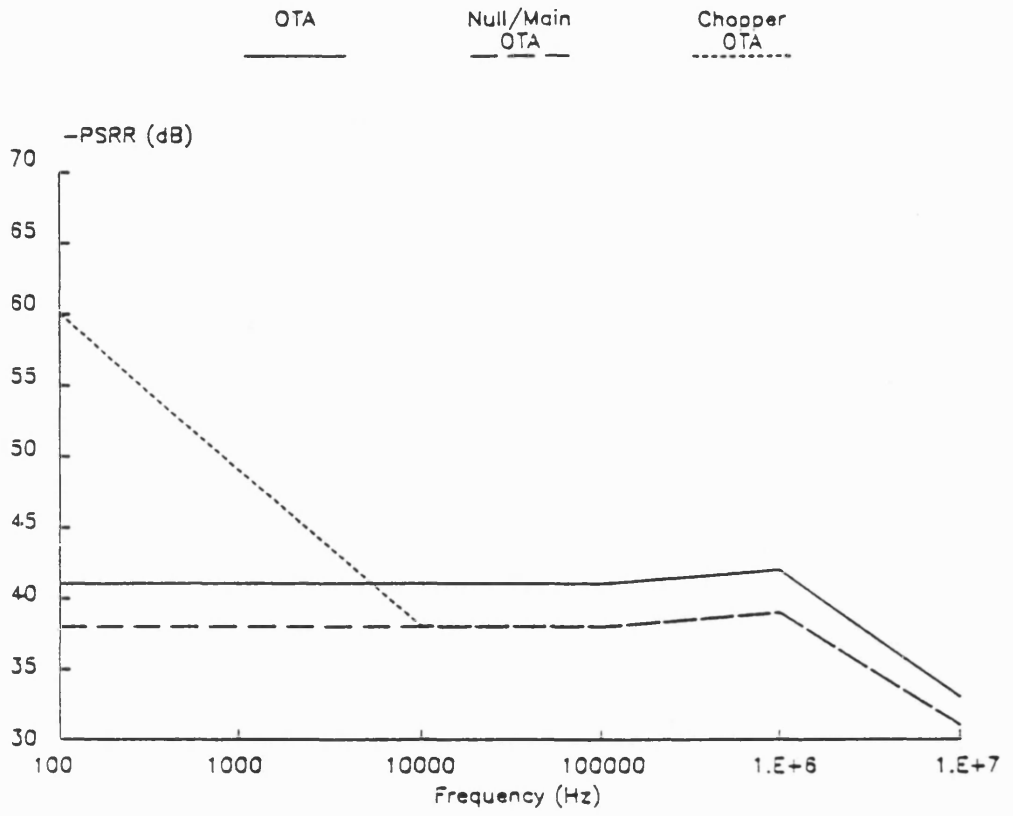


Figure 6. (*a*) Common mode rejection ratio. (*b*) Positive rail power supply rejection ratio. (*c*) Negative rail power supply rejection ratio.

The advantage of this design is the time-continuous operation of the main amplifier. The ability of a switched amplifier configuration to charge or discharge the appropriate circuit capacitances within a specified time is limited by the DC gain of the amplifier. Hence the design presented here can provide greater accuracy in SC circuits. Rejection of supply ringing is increased not only by the cascaded amplifier configuration, but also the dynamic biasing contributes to an improvement in PSRR and CMRR.

5. Summary

A monolithic chopper amplifier with a current controlled cascode output stage and a dynamic bias control has been presented which is applicable for use in high accuracy CMOS analogue designs. The amplifier incorporates offset voltage compensation and gives improved common mode and power supply rejection at low frequencies. The low pass filter built with a switched capacitor circuit enables the design components to be realised in silicon.

Acknowledgments

The authors would like to express their thanks to the Bosch Design Centre, Reutlingen, West Germany, for the use of the BONSAI simulator.

The support of the Nuffield Foundation is also gratefully acknowledged.

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Goldberg, E. A., 1950, Stabilization of wide-band direct-current amplifiers for zero and gain. *RCA Review*, June, 296–300.

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4M-545188/ELECTR/84846/1K5010

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Novel fully differential chopper OTA with dynamic bias control and current controlled cascoded output

W. J. TENTEN† and P. R. SHEPHERD†

A novel fully symmetric chopper operational transconductance amplifier (OTA) design is presented. This OTA concept improves the indirect chopper OTA design presented in a former paper in respect of higher CMRR, PSRR, clock feed through immunity and an increased slew rate. This amplifier is wholly realizable on silicon.

1. Introduction

A recent paper presented a novel chopper operational transconductance amplifier (OTA) using a current controlled cascode stage (Tenten and Shepherd 1988). Advanced circuit design techiques, especially in analogue-to-digital converters (ADCs), need high accuracy analogue building blocks to achieve resolutions beyond 14-bit. As shown in this first paper, the accuracy of standard OTA designs can be improved by using an offset compensation technique using the indirect chopper concept. The accuracy in switched capacitor (SC) circuits is limited by the clock feed-through error voltage induced by the switches. Minimizing these effects can be achieved by using a dummy switch at the positive input of the operational amplifier and additionally a cancelling capacitance of a magnitude that is the overall magnitude of all capacitances connected to the opposite amplifier input. Using this technique the resulting accuracy of these circuits is limited to ADC resolution of the order of 12 bits.

2. Circuit improvements

Following the design principle presented in the previous paper, the remaining clock feed-through error can further be minimized by using a fully differential operational amplifier in the indirect chopper technique. This concept needs two separate by-pass routes, as shown in Fig. 1. The offset compensation is achieved using an auto-zeroing cycle in each by-pass. The amplifiers used in the by-pass are called nulling amplifiers, because they are connected to the nulling inputs of the time continuous main amplifier via a low-pass filter. The low-pass filter shown in Fig. 2 is designed with a switched capacitor in order to make it realizable on silicon; the large R–C constant would make it impractical to realize with an actual resistor. Here the differential input section including the nulling input stage, separated by an individual bias supply, symmetrically supplies both output stages. To achieve a symmetric control on both sides, a reverse stage is used to shift the control level used for the n-channel output transistor. The bias control current cascode stage is used to control the output cascode transistors. The biasing can be done either by using a constant current source, such as a Widlar source, as shown in Fig. 3, or by using a

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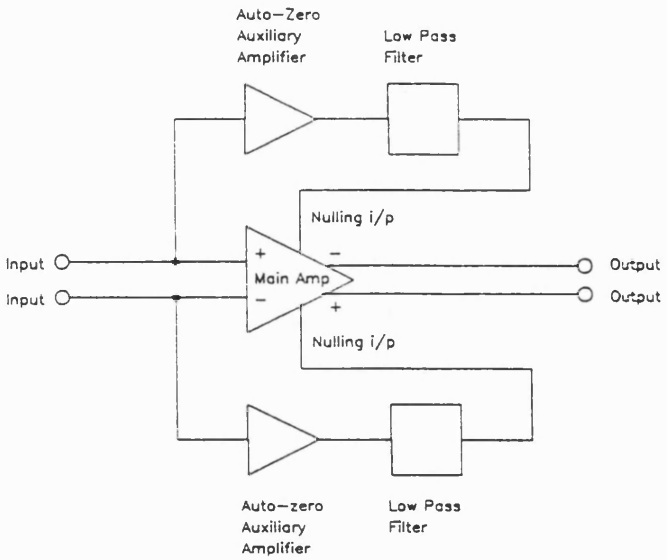

Figure 1. Block diagram of differential chopper OTA.

dynamic current source as shown in Fig. 4. It is to be noted that using the dynamic current control, the energy drawn by the bias source during the active time must be equivalent for both current sources. Figure 5 shows the block diagram of the fully differential chopper OTA including the SC low-pass filter section.

3. Simulation results

The overall resolution of the system is increased with the additional amplification of the nulling amplifier. Expressions for the signal amplification, the power supply rejection ratio (PSRR) and the common mode rejection ratio (CMRR) have been derived by Hsieh *et al.* (1981). The noise is also improved using this cascaded chopper concept with a fully differential OTA design technique.

The simulation tool used in this work is BONSAI (Bosch Network Simulation and Analysis Instrument). BONSAI is a network analysis simulator with parametric

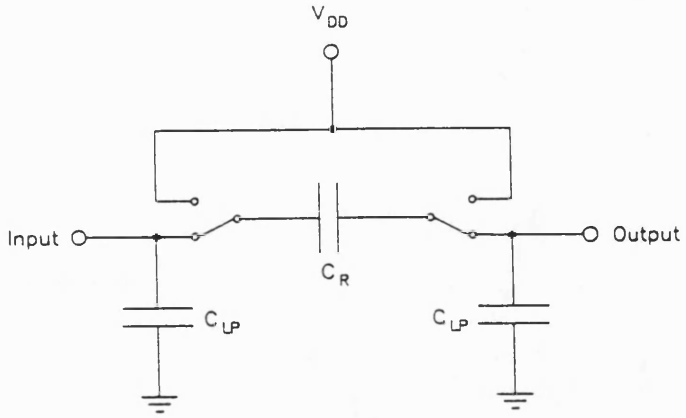

Figure 2. SC low-pass filter.

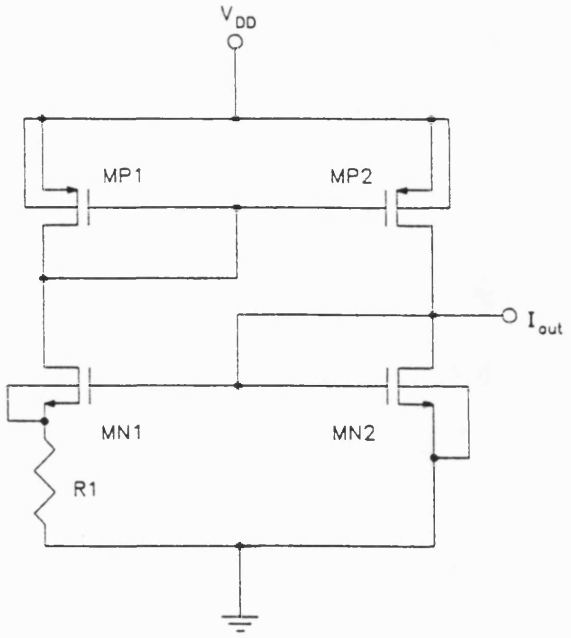

Figure 3. Widlar current source.

model equations. The parameters being used are based on the semiconductor physics of the devices. Analysis can be performed under DC, transient, or AC conditions. Transient simulations are based either on state variable analysis (SVA) or modified nodal analysis (MNA). SVA operates faster than MNA and is especially

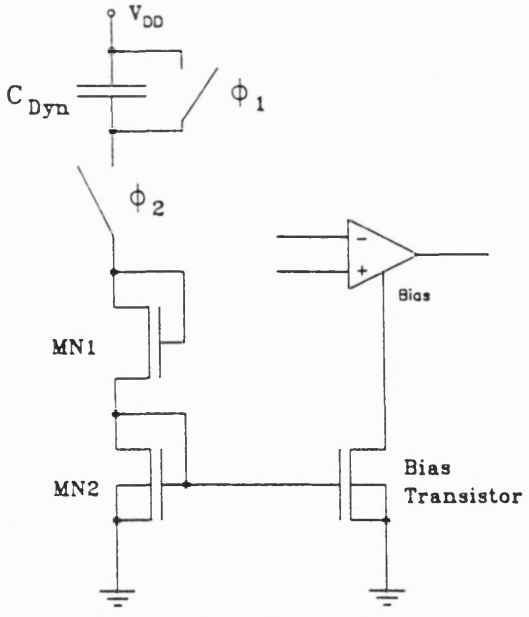

Figure 4. Dynamic current source.

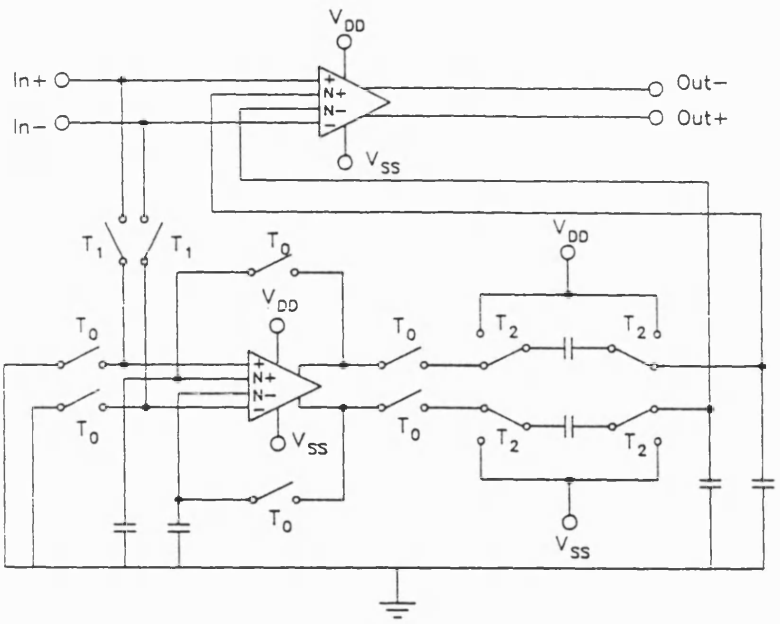

Figure 5. Fully differential chopper OTA.

applicable for digital simulations. MNA is more useful if the nodes are connected with large conductances and/or capacitances and the conductances/capacitances to ground are small. It has been found that BONSAI has greater mathematical stability compared to other tools, e.g. SPICE.

BONSAI has an automatic time-step adjustment mechanism, whereby the step-width is reduced if any nodal voltage changes faster than a preset error value. Owing to this, the simulation times for large circuits can become excessively long. Therefore, it is often better to split a particular circuit into several sub-circuits for analysis, and then use the results from one sub-circuit as the initial values for the simulation of the next sub-circuit. This can lead to dramatic savings in CPU time. Some of the simulations of the fully differential chopper OTA presented here were carried out using a series of sub-circuits. The sub-circuits are now described.

Parameter	SOTA	CSOTA
Supply voltage (V)	5	5
Common-mode range (V)	V_{th} to $V_{SS}-V_{th}$	V_{th} to $V_{SS}-V_{th}$
Slew rate $(V\,\mu s)^{-1}$	25	25
Minimum load capacitance (pF)	20	20
Unity gain frequency (MHz)	15	15
Phase margin (degrees)	20	20
$CMRR_{DC}$ (dB)	73	133
$PSRR_{DC}$ V_{DD} (dB)	39	96
$PSRR_{DC}$ V_{SS} (dB)	38	96
A_{DC} (dB)	60	115
F_{chop} (Hz)		500
F_{sc} (Hz)		4000
V_{off} (mV)	10	<0·05

OTA parameters.

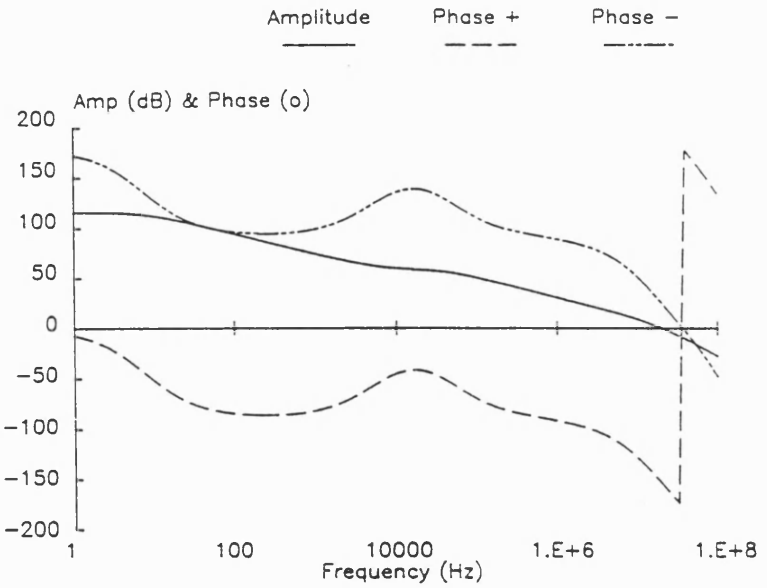

Figure 6. Amplification characteristics.

(*a*) *Symmetric OTA (SOTA).* Basic SOTA with current controlled cascode but without dynamic biasing.

(*b*) *Chopped symmetric OTA (CSOTA).* Based on (*a*) but using the indirect chopper principle. The low-pass filter is made up of an RC network.

(*c*) *Bias.* Constant and dynamic bias sources.

(*d*) *Low pass.* SC realisation of the low pass filter.

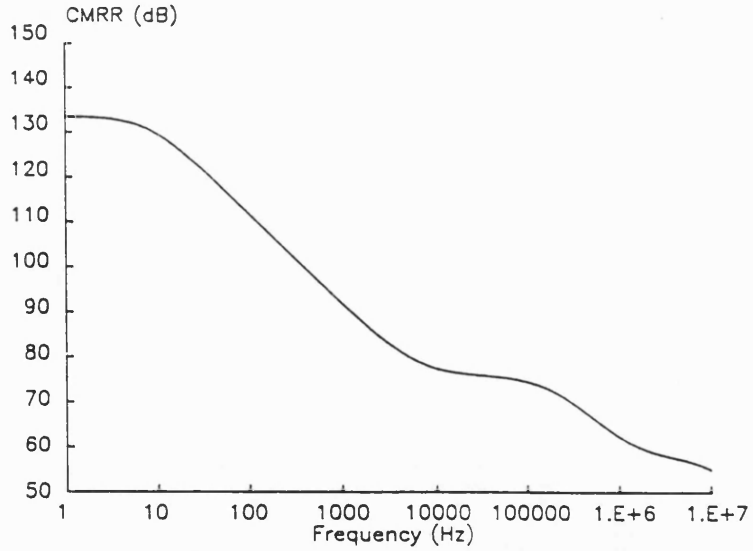

Figure 7. Common-mode rejection ratio.

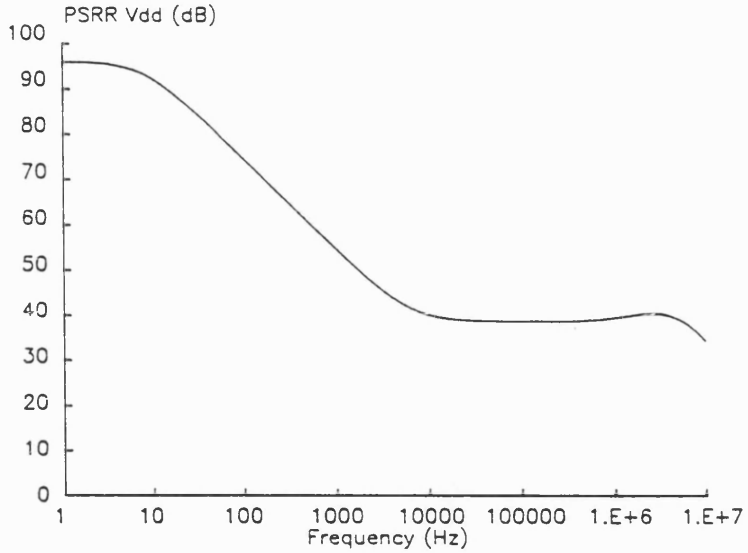

Figure 8. Power supply rejection ratio (V_{DD}).

A summary of results of the BONSAI simulations of the CSOTA is given in the Table. The results for the AC characteristics, i.e. amplification, CMRR and PSRR are presented in graphical form in Figs 6–9.

4. Discussion of results

The stacked characteristics of the indirect chopper design show a dramatic increase in the quality of the small signal parameters below the corner frequency induced by the low-pass filter of the nulling amplifier section. An additional

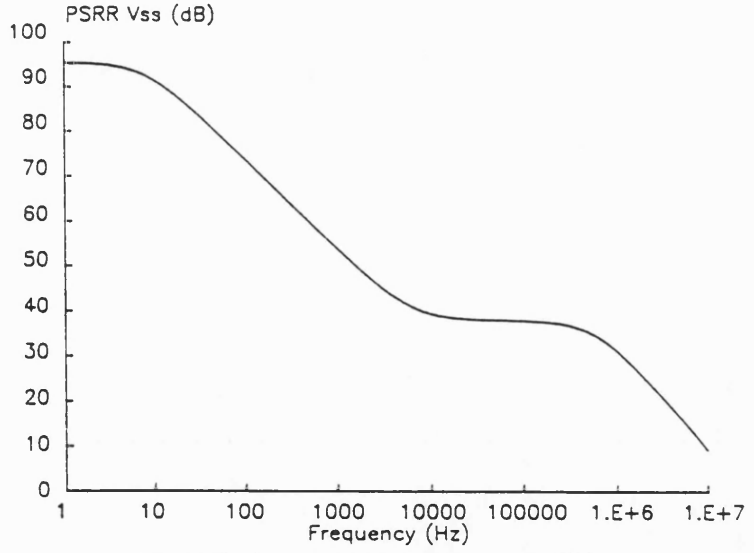

Figure 9. Power supply rejection ratio (V_{SS}).

improvement can be seen using the fully differential chopper OTA in the CMRR range (Fig. 6). The standard application frequency range used in A/D converters operating in sensor control units or in speech processing is below 20 kHz. Hence the clock feed-through applied symmetrically on both inputs will be damped by the high CMRR value. Improvement of the CSOTA shifts the resolution in the range up to 16 bits using fully symmetrical A/D converters. The clock feed-through induced by the switched capacitor low-pass filter is reduced by using a big low-pass capacitance ($C_{null} = 100\,pF$) and is additionally reduced by the fully symmetrical clock. Hence the clocks needed to control the nulling amplifier will be damped by the low-pass filter. Additionally, $1/f$ noise reduction is seen, according to the description presented by Hsieh *et al.* (1981).

5. Summary

A monolithic, fully symmetrical, chopper OTA using a bias current controlled cascode output stage and the possibility of choosing either a constant bias source or a dynamic bias source has been presented. This amplifier deisgn is particularly useful in the field of analogue-to-digital conversion in speech processing systems or in controlling sensor signals. The amplifier incorporates improved offset compensation techniques, PSRR, CMRR, gain and minimization of clock feed-through error voltage. The low-pass filter built with a switched capacitor circuit enables this design to be realized in silicon.

Acknowledgments

The authors would like to express their thanks to the BOSCH microelectronic centre, Reutlingen, West Germany, for the use of the BONSAI simulator.

The support of the Nuffield Foundation is also gratefully acknowledged.

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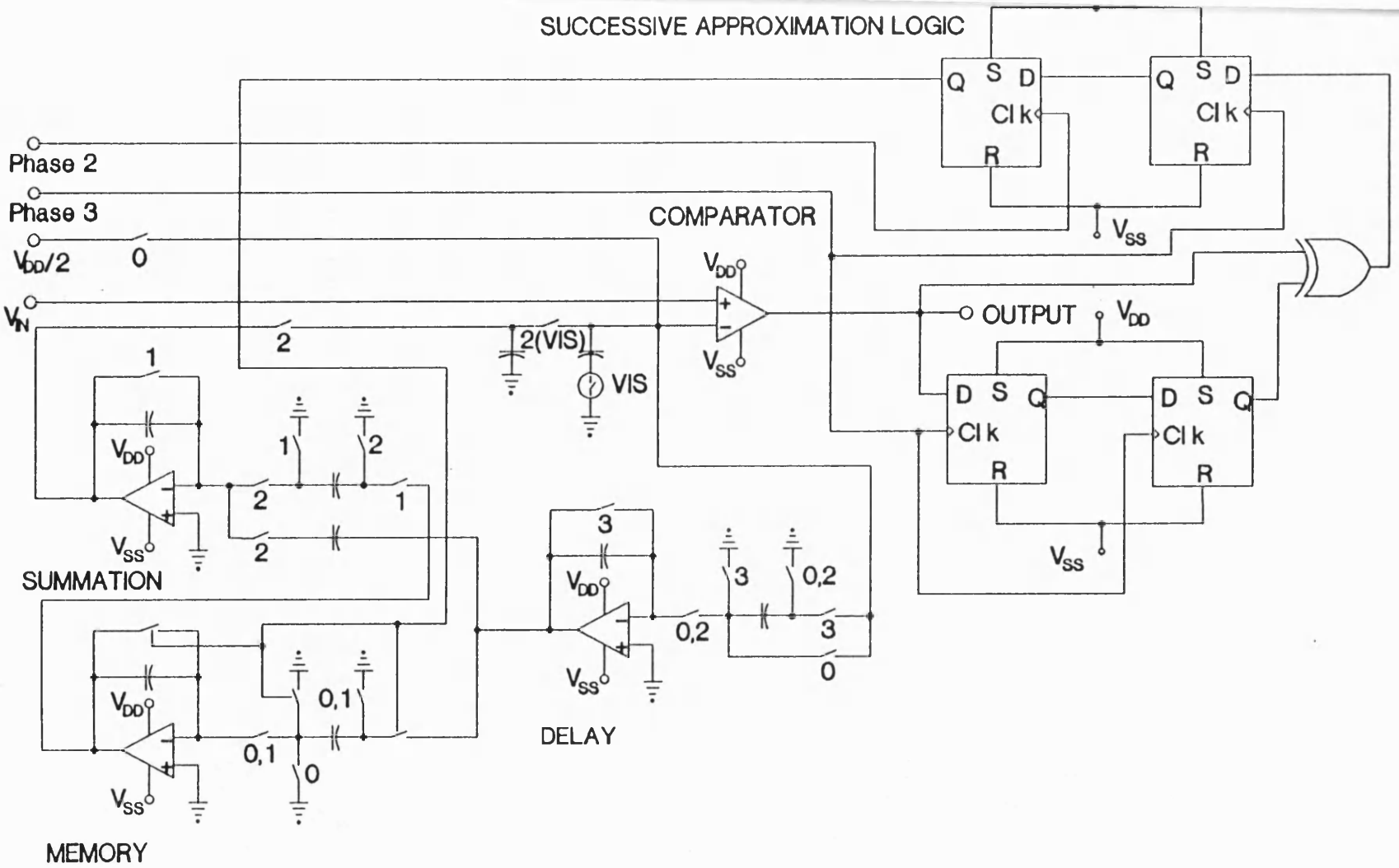

Figure 1. Successive Approximation VIS Controlled ADC

A NEW CMOS HIGH-SPEED, HIGH ACCURACY AUTO-ZERO COMPARATOR DESIGN BASED ON SYMMETRIC CROSS COUPLED CONCEPTS

ABSTRACT

Based on standard auto-zero techniques, a new design of CMOS comparator is presented. The amplifier offset and the clock feed-through offset of the switches are cancelled using a fully symmetric design and layout. Speed and accuracy improvements are gained from using a cross-coupled capacitor configuration.

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Short title : A SYMMETRIC CROSS COUPLED CMOS COMPARATOR.

1) BACKGROUND

One particular difficulty encountered in the design of comparator circuits is that of the input offset voltage. For precision applications such as high resolution A/D converters, any remaining offset voltage can severely limit the circuit operation. A technique which has proved useful in counteracting offset effects is that of auto-zeroing (Allen & Holberg 1987). This technique is particularly useful in MOS circuits due to the very low leakage capacitors that may be realised, which enable voltages to be stored for long periods of time. Therefore offset voltages can be sampled and held on a capacitor and then summed with an input voltage so as to cancel the offset.

This approach leads to the auto-zero technique, which is a two-stage process, usually controlled by a non-overlapping two-phase clocking system. The first stage is the auto-zero stage (phase 1), and the second stage is the comparison stage (phase 2). In the auto-zero stage any offset voltages on the input of the comparator are sampled and stored on the capacitor. In this stage the comparator is configured to act as a unity gain buffer amplifier to charge the capacitor. In the comparison stage the comparator resumes its normal high-gain behaviour and the stored offset is summed with the input voltage so as to cancel the offset effects. The offset voltage is generally made up of the amplifier d.c.-offset voltage and also clock feed-through voltages (Allen & Holberg 1987).

Based on these standard auto-zero techniques, this paper describes a new auto-zero comparator design which incorporates a symmetric cross-coupled configuration. Improvements in the standard auto-zero techniques are described which can improve the resolution of the comparator. Further improvements are obtained by minimising the residual offset effects with the aid of the symmetric cross-coupled design. Both switched cross-coupling and capacitor cross-coupling are examined.

2) AUTO-ZERO COMPARISON ROUTINES

The two phases of the auto-zero routine are shown in Figs. 1a and 1b respectively. The switches S_1 and S_2 are controlled by the two-phase clock. C_a is an auxilliary capacitor for storing the offset voltages and C_i is the input capacitance of the inverter. In the ideal case, the reference voltage will be stored on C_a in the first phase. The input voltage is then applied in phase 2, the offset is cancelled, and the output of the comparator depends solely on the sign of the difference between V_{ref} and V_{in}. In reality the offset will not be completely cancelled due to the finite input capacitance, limited gain of the amplifier, resistance of the transfer gates, etc. A more detailed analysis of this routine is given below.

In this first phase, Fig. 1a, switch S_1 is connected to V_{ref} and switch S_2 is closed making the inverter circuit into a nominally unity gain buffer amplifier. The input voltage to the amplifier has a number of components. It is normally biased to the mid-point voltage of the supply rails, in CMOS circuits this is given by $\frac{V_{dd}+V_{ss}}{2}$. The offset voltages consist of the amplifier d.c.-offset voltage $V_{off,amp}$ and an offset due to clock feed-through, $V_{off,cft}$. These terms can be grouped together to give a total offset voltage, V_{off}.

$$V_{off} = \frac{V_{dd}+V_{ss}}{2} + V_{off,amp} + V_{off,cft}$$

This voltage effectively appears across the input capacitance C_i, therefore the voltage stored on C_a during this phase is $-(V_{ref}+V_{off})$.

ii) Phase 2 : Comparison.

In this phase, Fig. 1b, S_1 connects V_i to the comparator, and S_2 opens, converting the amplifier into its normal high gain mode. Ideally the component V_{off} stored on C_a with V_{ref} cancels the V_{off} on the input to the comparator and the output of the inverter depends solely on the sign of $V_i - V_{ref}$.

However, if we look at the input circuit just after the switches are closed, Fig. 2, we see the effect of C_{ii}. V_x is the decision voltage, the sign of which determines the output of the comparator. The charge flow through C_a will be given by

$$q = \frac{C_a C_i}{C_a + C_i}(V_i - V_{ref} - V_{off})$$

Hence V_x will be given by

$$V_x = \frac{C_a}{C_a + C_i}(V_i - V_{ref} - V_{off})$$

V_{off} will be added internally to this applied voltage, so the offset will only be completely cancelled when $C_i \to 0$. We can improve the offset cancellation by making the $C_a >> C_i$, however this is at the cost of speed of the circuit.

This situation can be improved by having a cascade of three inverters to increase the current sourcing capability (Fig. 3). This enables the auxilliary capacitors C_a, C_b, and C_c to be made increasingly large without excessive speed penalties. This is a very similar technique to that used in digital circuits for driving large capacitive loads. The overall comparator has of course a much larger gain which is an added advantage. However, this scheme requires more circuitry and a more complex timing system for the switches, as shown in Fig. 4.

The effects of finite amplifier gain, clock feed-through from the transfer gates, and their resistance, are now described. These effects mean that the amplifier in the high gain mode has a finite gain, A_0, and in the auto zero mode, it has a non-ideal (not exactly unity) gain of A_{az}. There will also be a certain amount of clock feed-through from the switching of the transfer gate S_2. Taking all these effects into account, the output voltage of the compensated inverter will be :

$$V_o = -A_0(V_i - V_{off}) - A_{az} V_{az}$$

where V_{az} = the residual auto-zero offset voltage resulting from clock feed-through. The first term on the RHS of (4) shows the normal offset voltage which will be largely cancelled by the auto-zero technique described above. The second term is a residual effect which is not taken into account by the auto-zero technique.

Using these auto-zero techniques, A/D converters can be realised with 10-bit resolution. However, these circuits still suffer from the residual clock feed-through errors and also poor rejection of power supply ringing. To achieve 12 bit resolution the sensitivity to these effects must be improved. This can be done by using symmetric cross coupled comparator circuits. Two possible circuits are examined - switch controlled and capacitor controlled.

3) THE SWITCH-CONTROLLED CROSS COUPLED COMPARATOR

The idea of symmetric comparator circuits has been proposed in the past. (Scott et al. 1986), (Chin et al. 1981), (McCaroll et al. 1988), whereby the operational amplifier inputs are symmetrically designed to minimise offset voltages and achieve higher resolution. Ng & Salama (1986) introduced a cross-coupled latch circuit which was applied to a comparator. Cross coupling can further reduce the residual offset voltages. In fact the latch circuit itself can act as a comparator, as shown in Fig. 5.

The operational phases correspond to those of the auto-zero comparator described in the previous section. In phase 1, each inverter is offset calibrated by closing the auto-zero switches. The two halves of the circuit act independently, with the cross coupled switches opened. The cross switches remain open at the start of phase 2, so each inverter acts independently until the output voltage of each amplifier is large enough to avoid erroneous decisions from clock feed-through of the cross-coupled switches. These switches are then closed, increasing the loop gain and causing the circuit to latch to the correct output voltage. The buffer inverters are required to drive the output capacitive loads and to maintain the circuit symmetry by ensuring the nodal capacitances of nodes 1 and 2 are

virtually identical.

4) THE CAPACITOR CONTROLLED CROSS-COUPLED COMPARATOR

In fact the circuit described in the previous section can be simplified and improved by substituting capacitors for the cross-coupling switches, as shown in Fig. 6. The advantages of this circuit is that the third clocking sequence to control the cross-coupling switches, T_1, is no longer required, and there is no clock feed-through effect from these switches. The substitution of capacitors for switches is valid, since the switches are activated once the output voltage has reached a certain level. This is identical to an appropriate charge having flowed to control the parallel circuit.

The size of the cross-coupling capacitors must be designed correctly such that they are large enough to avoid sensitivity to residual offset voltages, without too great a delay in the clocking cycle. In practise the cross-coupled capacitors are about ten times the value of the input capacitors.

5) SIMULATION RESULTS

The simulations of the comparator circuits were performed using DEMONA. (Herbst et al. 1987), a computer package based on the modified nodal analysis. It employs transistor, capacitor and resistor models based on the physical properties of the devices to simulate small scale analogue circuits. Previous results have shown very good agreement between theoretical and measured results.

Figs. 7a and 7b show the simulation results for the capacitor controlled cross-coupled comparator for $V_i - V_{ref}$ = 1 mV and -1 mV respectively. The solid line in the two plots is the clock waveform T, $\bar{T}$ being the inverse of this clock. The dotted curves represent the voltage at node 1, and the broken curves the voltage at node 2. The correct comparator decision with a difference of 1 mV using a 5V power supply indicates a resolution of 12 bit in A/D converter applications.

The clock feed-through spikes of the input switches can be seen in Figs. 7a and 7b at the start of the active clock period. The feed forward effect of the cross-coupled capacitors can be seen as a small delay in the output node voltages after the rising edge of the active clock. This shows that the clock feed-through spike does not influence the decision of the comparator.

The capacitor controlled circuit shows a very good compromise between high resolution (of the order of 12 bit), high speed (comparison times of 50-60 nsec) and good sensitivity to clock feed-through effects. The auto-zero time is very dependent on the size of the transfer gates. From the

point of view of resistance of the switches, very wide devices are required.

a largee nodal capacitance, which increases the auto-zero time, typically about 200 nsec for the 1 mV reesolution. This is a function of the residual charge just before the comparison period, which must tbe an order of magnitude lower than the specified resolution.

6) CONCLUSIONS

A novvel auto-zero comparator has been described which uses a symmetric layout and a cross couplling technique to minimise the effects of residual offset voltage. a good compromise has been demonstrated between high resolution, high speed and circuit complexity. The circuit has low sensittivity to clock feed-through effects and power supply ringing due to the symmetric design and layowt. If used in an A/D converter system, a theoretical resolution of 12-bit has been demconstrated.

ACKNOWLEDGEMENTS

The authors would like to thank Drs. Dieter Herbst and Hans Sibbert for use of the simulation proggram DEMONA. The support of the Nuffield Foundation is also gratefully acknowledged.

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LIST OF ILLUSTRATIONS

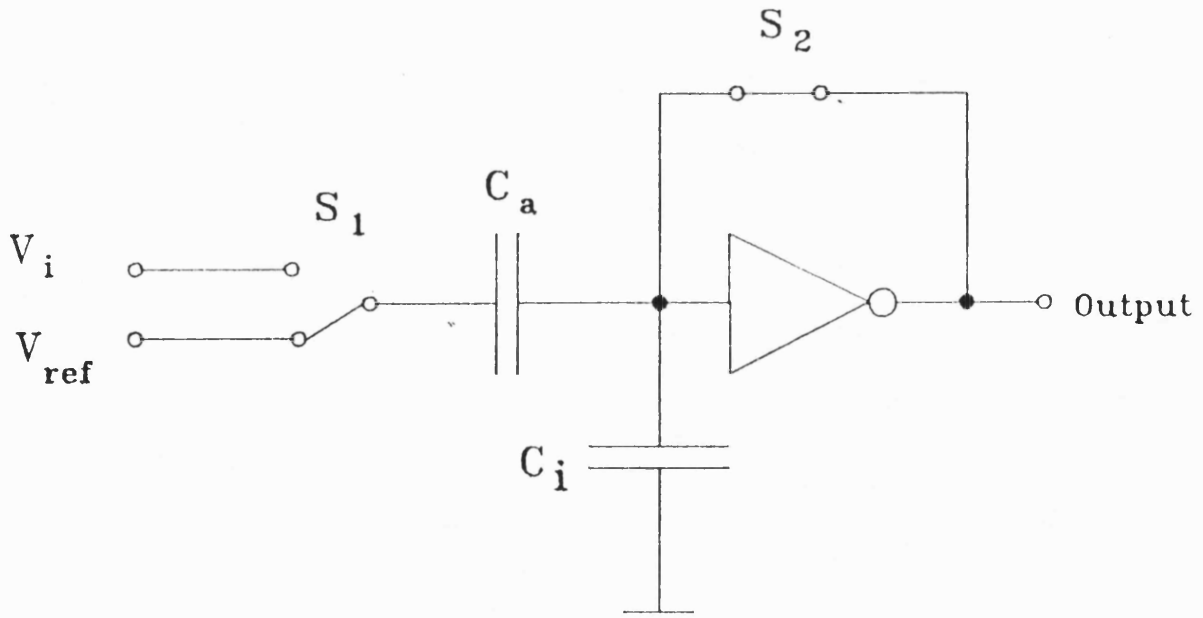

Figure 1a. Phase 1 of the auto-zero comparison

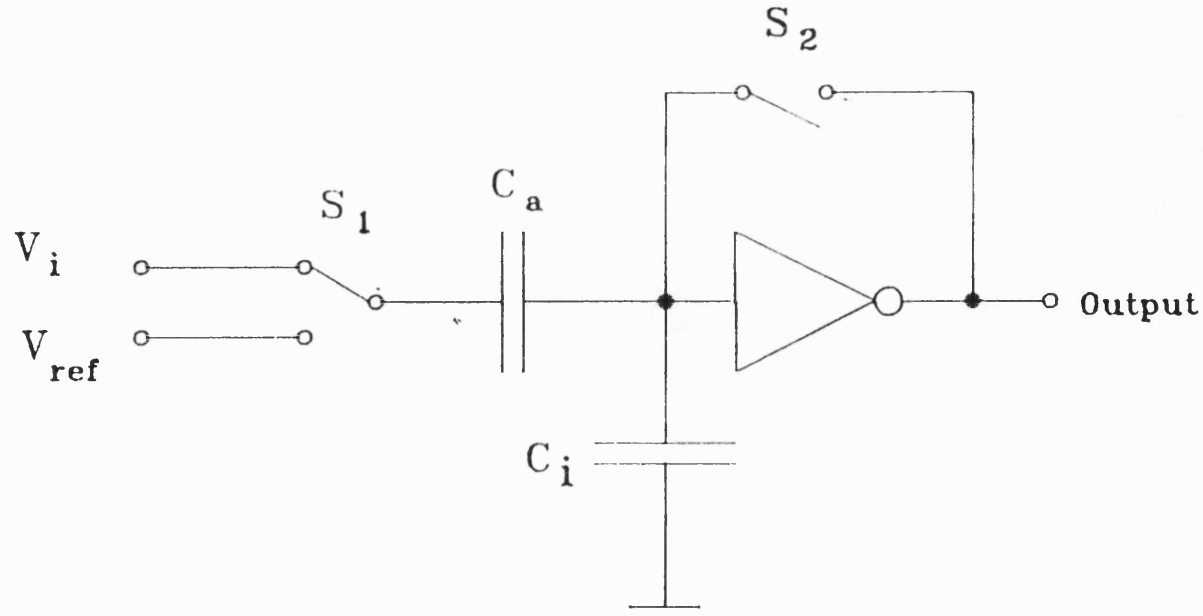

Figure 1b. Phase 2 of the auto–zero comparison

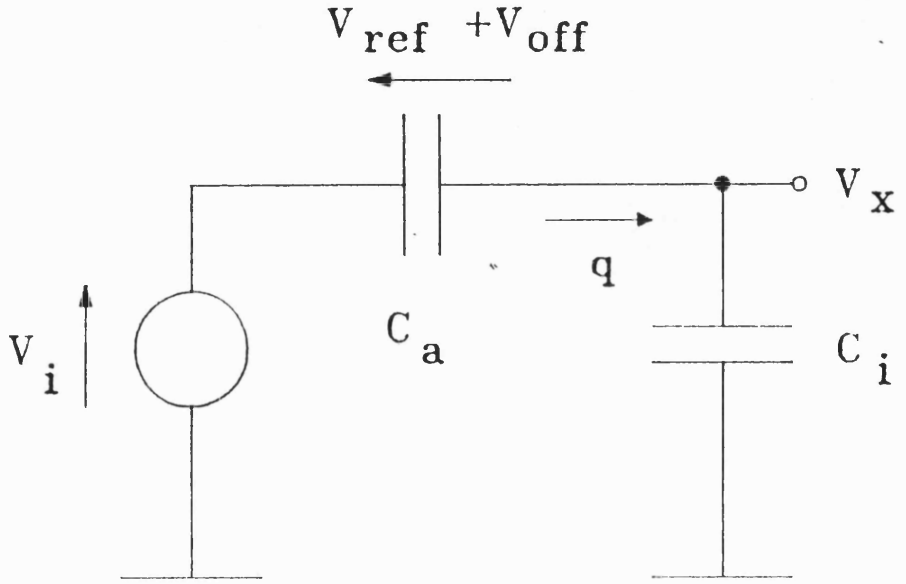

Figure 2. Input circuit at beginning of comparison phase

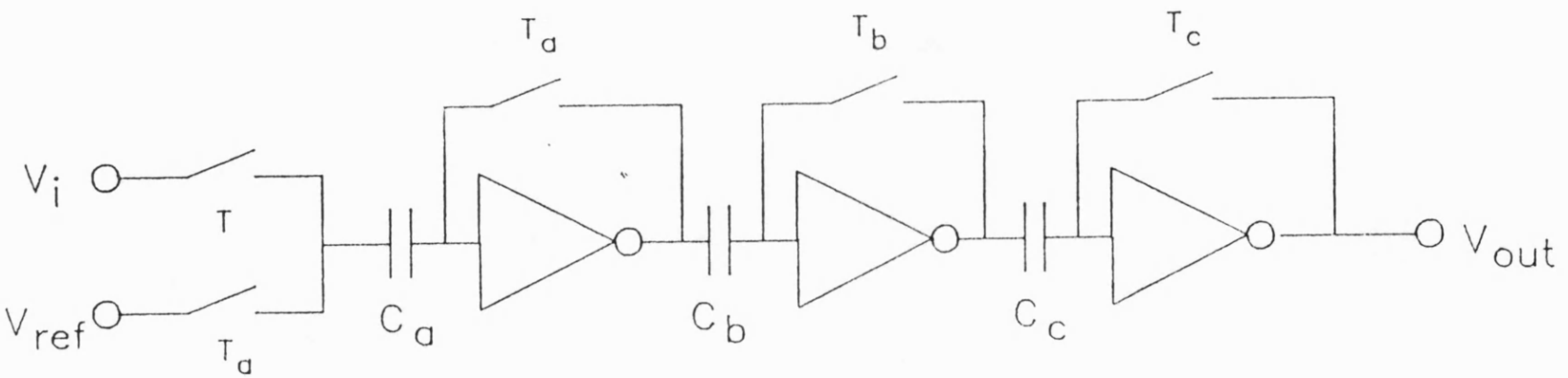

Figure 3. Three-stage auto-zero comparator

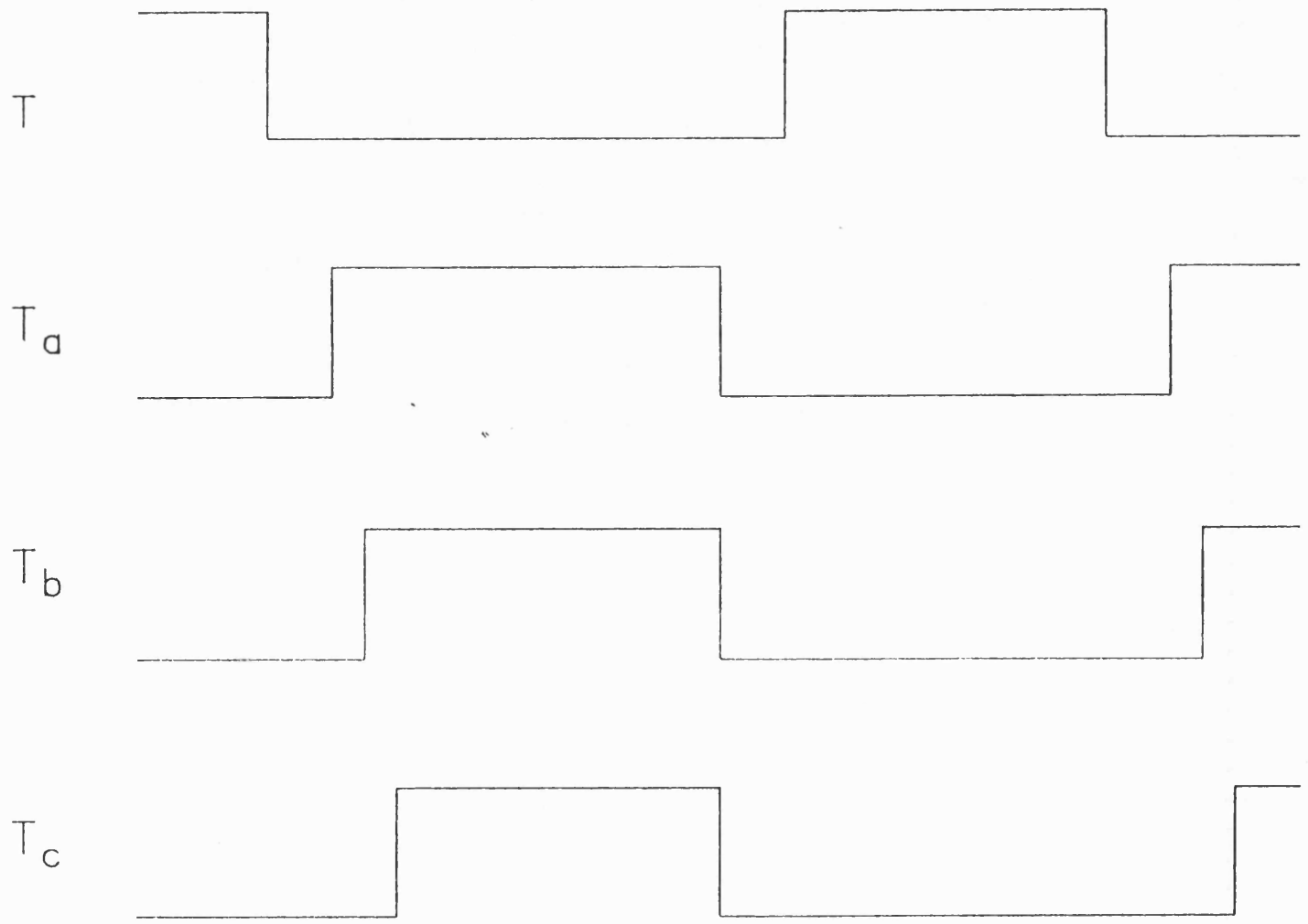

Figure 4. Three–stage comparator timing diagram

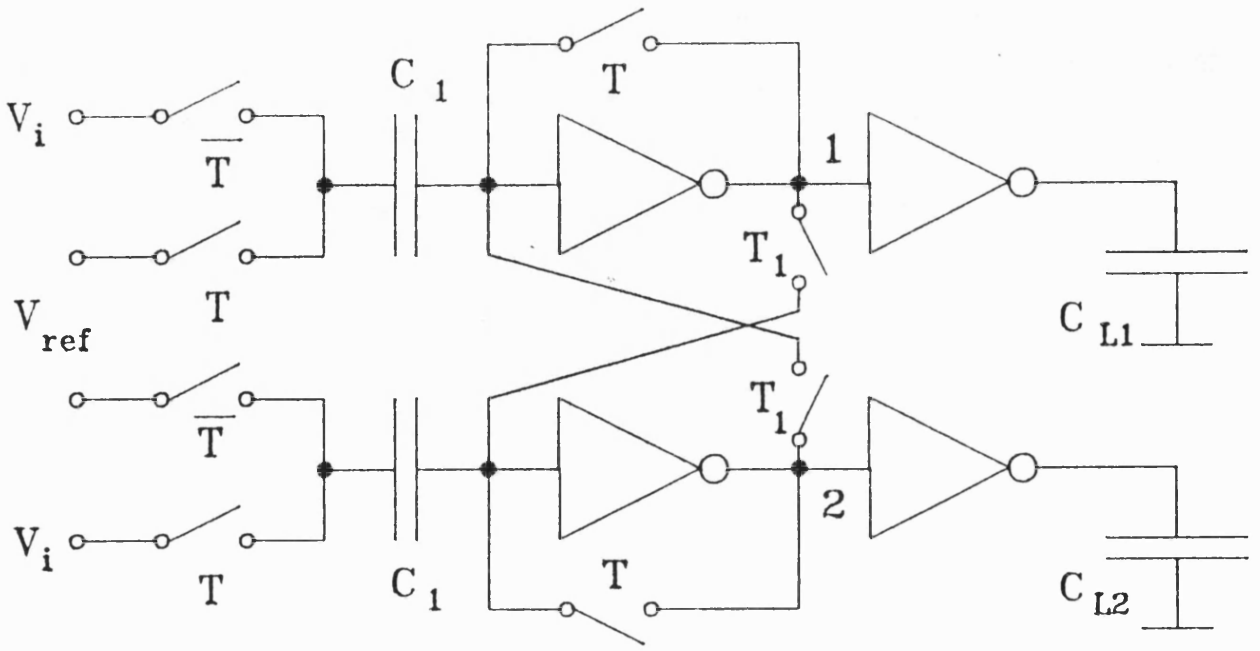

Figure 5. Switch Controlled Cross Coupled Comparator

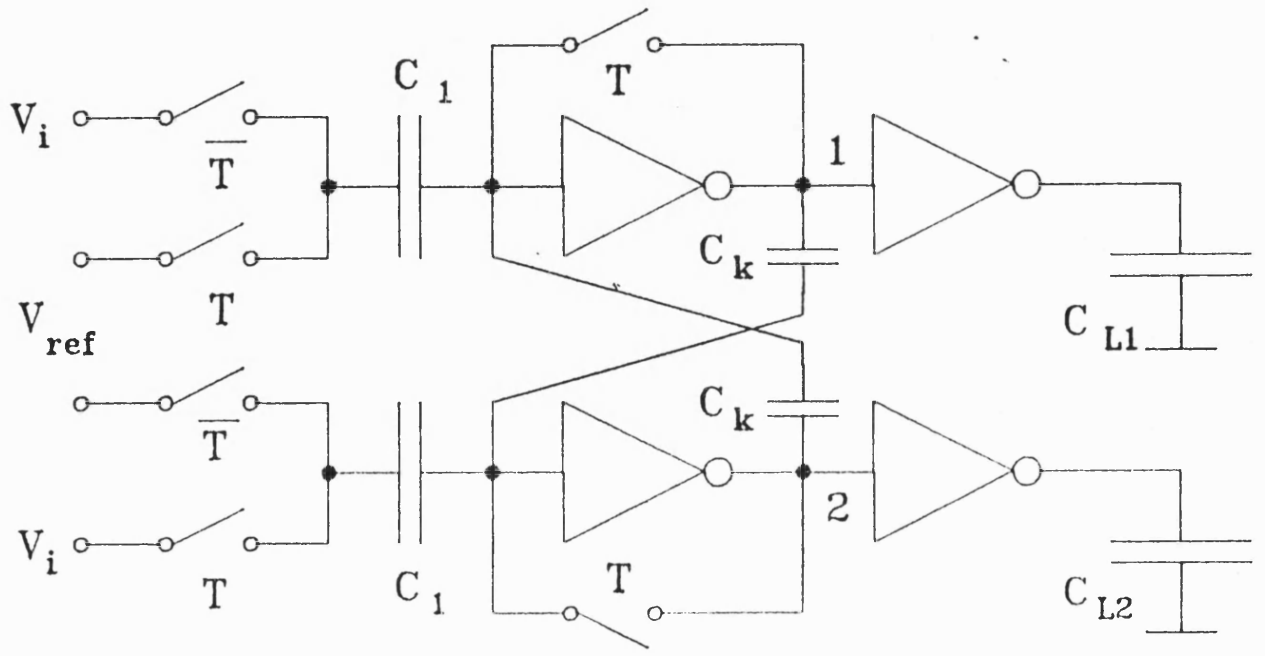

Figure 6. Capacitor Controlled Cross Coupled Comparator

Figure 7a $V_{in}-V_{ref}$ = 1mV

——— clock voltage

..... node 1 voltage

------ node 2 voltage

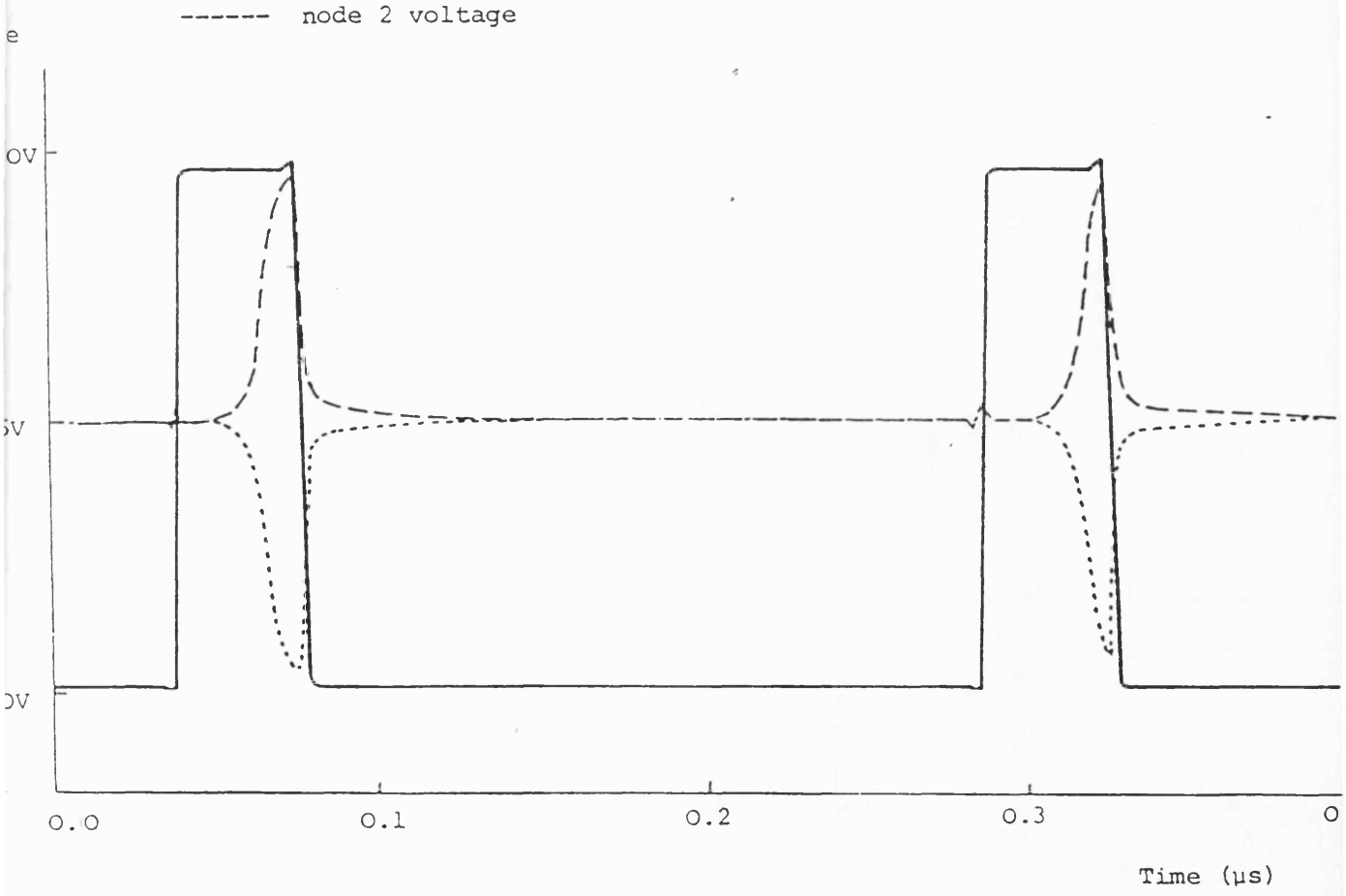

Figure 7b $V_{in}-V_{ref}$ = -1mV

——— clock voltage

..... node 1 voltage

------ node 2 voltage